CONVERSION GAIN AND INTERPIXEL CAPACITANCE OF CMOS HYBRID FOCAL PLANE ARRAYS

Nodal capacitance measurement by a capacitance comparison technique

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Abstract:

The conversion gain of optical and infrared focal plane CMOS hybrid arrays is a fundamental parameter, whose value enters into the derivation of other parameters characterizing the performance of a detector. The widespread “noise squared versus signal” method used to obtain the conversion gain can overestimate the nodal capacitance of the detector pixel by more than 20% for infrared arrays and by more than 100% for Si-PIN diode arrays. This is because the method does not take account of the capacitive coupling between neighboring pixels. A simple technique has been developed to measure the nodal capacitance directly by comparing the voltage change of an external calibrated capacitor with the voltage change on the nodal capacitor of the detector pixel. The method is elaborated in detail and has been verified with a Si-PIN diode array hybridized to a Hawaii-2RG multiplexer using an Fe^{55} X-ray source. It is also in good agreement with a stochastic method based on 2D autocorrelation.

Key words: conversion gain, interpixel capacitance, CMOS hybrid, quantum efficiency, HgCdTe, Hawaii-2RG, Si-PIN

1. INTRODUCTION

The measurement of the quantum efficiency (QE) of CMOS hybrid arrays recently produced implausible efficiencies exceeding 100%. Many factors such as radiation geometry, blackbody calibration, temperature dependence of the filter transmission, and filter leaks may contribute to this problem[1]. During characterization of infrared arrays, we have tried to reduce the errors of each of the factors listed above without succeeding in obtaining a quantum efficiency in K-band of a λ_c=2.5μm HgCdTe Hawaii-2RG array below 105%.

The remaining major uncertainty in our QE measurements was the conversion gain, C_0/e, measured in units of electrons per millivolt. The nodal capacitance C_0, which is the capacitance of the integrating node, is composed of the voltage dependent diode capacitance of the detector pixel and the fixed gate capacitance of the unit cell source follower gate. The nodal capacitance of CMOS hybrids has, until now, usually been determined by the widely used shot noise method that assumes photon shot noise limited performance of the detector. Photons are governed by Bose-Einstein statistics. If the photon energy is small compared to kT (k is the Boltzmann constant and T is the absolute temperature of the radiation source), the variance of the integrated number of photons is equal to the mean number of photons. In this case, the nodal capacitance C_0 can be calculated from the slope of the plot of noise squared signal versus mean signal according to Eq. (1). However, this equation only holds true if the signals of neighboring pixels are uncorrelated as explained in section 3.

$$C_0 = e\frac{\langle V \rangle}{\langle V^2 \rangle} \tag{1}$$

2. CAPACITANCE COMPARISON METHOD

In order to obtain the nodal capacitance C_0 by a direct measurement which does not rely on statistical methods, a simple technique has been developed. This technique compares the voltage change of a large calibrated external capacitor to that of the unknown nodal capacitance C_0, which is many orders of magnitudes smaller.

During normal operation the reset voltage, V_{reset}, is connected to an external bias voltage of the detector control electronics and the bias provides the charge required to reset the integrating node capacitor. The hardware setup for the capacitance comparison simply entails adding a switch (relay) between the bias and V_{reset} and adding a calibrated capacitor, C_{ext}, between V_{reset} and detector substrate voltage D_{sub} as shown in Figure 1. The external capacitor is charged to the nominal reset voltage and disconnected (using the relay) from the external bias. The charge to reset the nodal capacitor C_0 of each pixel slowly discharges the external capacitor, C_{ext}. If the 2Kx2K pixels of the detector are exposed to a high photon flux and several frames are read out and reset, the charge to repeatedly reset the complete array will discharge C_{ext}, generating a voltage drop across C_{ext} large enough to be accurately measured.

$$\Delta V_{ext} C_{ext} = \sum_{n=1}^{n_{frames}} \sum_{i=1}^{2048} \sum_{j=1}^{2048} V_{n,i,j} C_0 \qquad (2)$$

Since the voltage drop ΔV_{ext} on C_{ext} and the signals of each pixel $V_{i,j}$ are known, the nodal capacitance C_0 and thus the conversion gain C_0/e can be calculated as shown in Eq. (2).

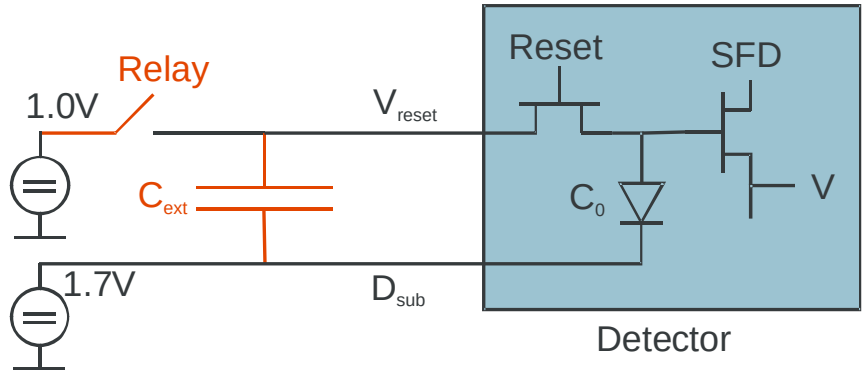

Figure 1. Hardware setup for capacitance comparison method for the measurement of the conversion gain

A capacitance of 9.26 µF was used for C_{ext}. It is much larger than the sum of the capacitance of all cables and other stray capacitances. The

capacitances of these components may therefore be neglected. Low leakage current capacitors such as foil should be used for C_{ext} . Ceramic capacitors should be avoided. Filtering, antistatic and protection circuitry on V_{reset} should be removed or modified if they have large leakage currents. For example, the antistatic protection Zener diode on our preamplifier board next to the focal plane was removed because of its large leakage current. In addition, the ceramic capacitor of the lowpass filter for V_{reset} was replaced by a foil capacitor. No modification is needed for D_{sub}. Leakage currents do not affect D_{sub} as it remains connected to the bias voltage. V_{reset} was increased from the nominal 0.5V to 0.7 V to avoid charge loss due to switching transients of the reset clock which may turn on the on-chip protection circuitry

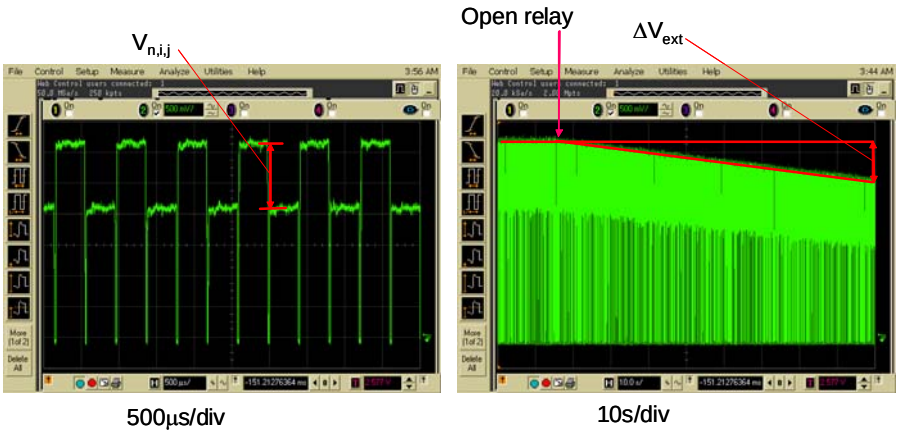

Figure 1. Oscilloscope traces of the detector signal while applying the capacitance comparison method. Left: detector signal in read-reset-read mode using line reset. Time resolution is 500 µs/division. All 64 pixels of a detector row are read at the end of the integration ramp, the row is reset and read again at the beginning of the next integration ramp. $V_{n,i,j}$ is the detector signal of the n^{th} frame of pixel (i,j). Right: same detector signal taken with time resolution of 10 s/division covering 50 frames. After the relay opens the DC level of the detector signal decreases due to the discharge of the external capacitor C_{ext}.

An example of the detector signal is shown in the oscilloscope traces in Figure 2. The detector is operated in read-reset-read mode using line reset. In the left image of Figure 2, the detector signal $V_{n,i,j}$, the n^{th} frame of pixel (i,j), is the difference between the voltages at the end of the integration ramp and the beginning of the next ramp immediately after applying the reset voltage which recharges the nodal capacitor of the detector pixel C_0. After charging the external capacitor C_{ext} and opening the relay, the charge to reset C_0 is

provided by C_{ext}. Consequently, the DC level of the detector signal slowly decreases (right side trace of figure 2) as the external capacitor C_{ext} is discharged. With increasing photon flux the discharge rate of C_{ext} increases.

The detector signal and its change in DC level can be observed by using the normal data acquisition chain operating the detector in the read-reset-read mode. By simply recording the raw data values before and after reset rather than the differences, as is normally done in double correlated sampling, both the pixel intensities and the DC level of the detector signal can be calculated. This is illustrated in Figure 3, which shows a small part of the array. The bright stripes are the pixels of the row read at the end of the detector integration. The dark stripes are pixels read immediately after reset and are the voltage V_{ext} on the external capacitor C_{ext}. The difference is the detector signal.

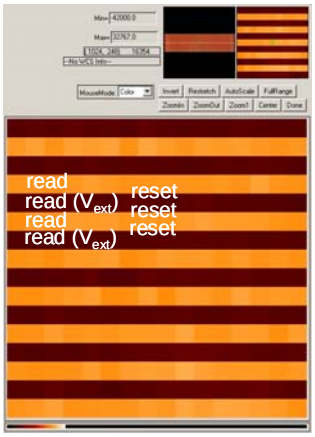

Figure 2. Read-Reset-Read: Bright stripes are pixels of a row read at the end of the integration. Dark stripes are pixels read immediately after reset and are the voltage V_{ext} on the external capacitor C_{ext}.

Depending on the photon flux to which the detector is exposed, the DC level of the detector signal drops at a proportional rate ΔV_{ext} /frame in ADU's per frame as shown in Figure 4. The number of frames can be selected to be sufficiently large to measure the voltage drop per frame ΔV_{ext} with the desired accuracy. This voltage drop is measured at different photon flux levels and plotted in Figure 5 versus the sum of the detector signal for the corresponding flux level. *(Note that each datum in Figure 5 comes from one slope of the measurements shown in Figure 4.)*

As shown by Eq. (2), the slope of ΔV_{ext} plotted versus the total detector signal $\sum V_{i,j}$ is equal to the ratio of the nodal capacitance and the external capacitance, C_0/C_{ext}. The external capacitor is 9.26 μF. Using the slopes from figure 5, the nodal capacitances of two different λ_c=2.5 μm HgCdTe arrays (Hawaii-2RG #13, Hawaii-2RG #66) and one Si-PIN array (HyViSI) hybridized to Hawaii-2RG multiplexers can be calculated.

The discrepancy of nodal capacitances C_0 determined by the capacitance comparison and the shot noise method is substantial (> 20 % for HgCdTe and more than a factor of two for Si-PIN arrays) as can be seen in Table 1.

device	Conversion gain capacitance comparison [e/mV]	C_0 capacitance comparison [fF]	C_0 shot noise [fF]
λ_c=2.5 μm HgCdTe Hawaii-2RG #13	201	33.5	40.9
λ_c=2.5 μm HgCdTe Hawaii-2RG #66	164	27.4	38.1
Si-PIN HyViSI Hawaii-2RG	86.8	13.9	28.5

Table 1. Comparison of nodal capacitances of CMOS hybrid arrays determined by capacitance comparison and shot noise method

Nodal capacitances obtained with the capacitance comparison method (Table 1) yields a quantum efficiency for the HgCdTe Hawaii-2RG array #13 in K-band of 86% instead of 105%, the value derived with the shot noise method. The shot noise method does not achieve plausible quantum efficiency using conversion gains derived from the standard “noise squared versus signal” technique.

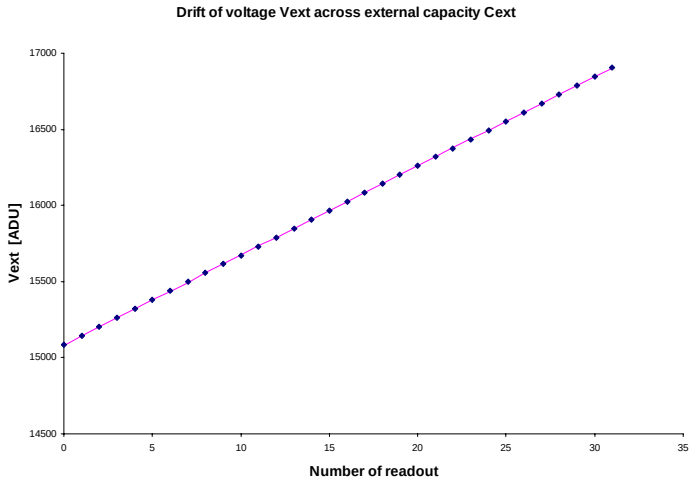

Figure 3. Drift of voltage V_{ext} across the external capacitor C_{ext} versus the number of detector integration. ΔV_{ext}=58.6 ADU/frame.

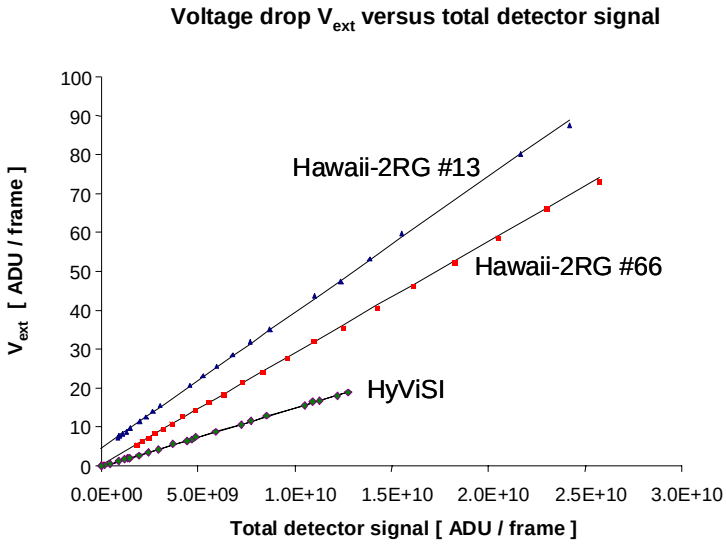

Figure 4. Voltage drop across the external capacitor V_{ext} versus the sum of the voltages of all detector pixels (-total detector signal) for the corresponding flux level. The total detector

signal is changed by increasing the photon flux on the detector. The slope of the least square fit is the ratio of the nodal capacitance and the external capacitance C_0/C_{ext} .

In an effort to compare and validate the two methods of deriving the conversion gain we used the K_α line of Fe^{55} which generates a well known number of electrons per absorbed x-ray photon and has been in use for many years to calibrate the conversion gain of optical CCDs[2]. Unfortunately, the Fe^{55} method cannot be applied to the HgCdTe double layer planar heterostructures of infrared arrays. The HgCdTe diode arrays of infrared detectors are grown by molecular beam epitaxy on a CdZnTe substrate which absorbs the x-ray rays of the Fe^{55} source and blocks them before they reach the depletion region of the infrared diodes. The CdZnTe substrates of HgCdTe arrays can be removed by chemical etching. For this type of HgCdTe arrays the Fe^{55} method can be applied, but ESO does not yet have such a device. For the Si-PIN diode array, however, the Fe^{55} calibration is applicable. A histogram showing the number of electrons generated by the absorption of one x-ray photon is shown in Figure 6. The solid curve represents the histogram generated using the nodal capacitance C_0 determined by the capacitance comparison method; the dashed curve shows the histogram of the same data set but using the nodal capacitance determined by the standard photon transfer curve technique. The accepted value[1] used in calibrating CCDs is shown as a vertical line in figure 6. (K_α x-rays generate an average of 1620 electrons in silicon.) It is evident that the capacitance comparison method is consistent with the Fe^{55} value cited in literature. The limitations of the applicability of the shot noise method using "noise squared versus signal" have to be investigated and a more thorough interpretation of the method is required.

The Fe^{55} method can also be applied to InSb detectors which do not have a detector substrate. First measurements yield a value of 2500 electrons per absorbed K_α x-ray photon. Possibly, the Fe^{55} method will also be applicable to HgCdTe arrays, if their substrate is removed. Further development in this area is needed.

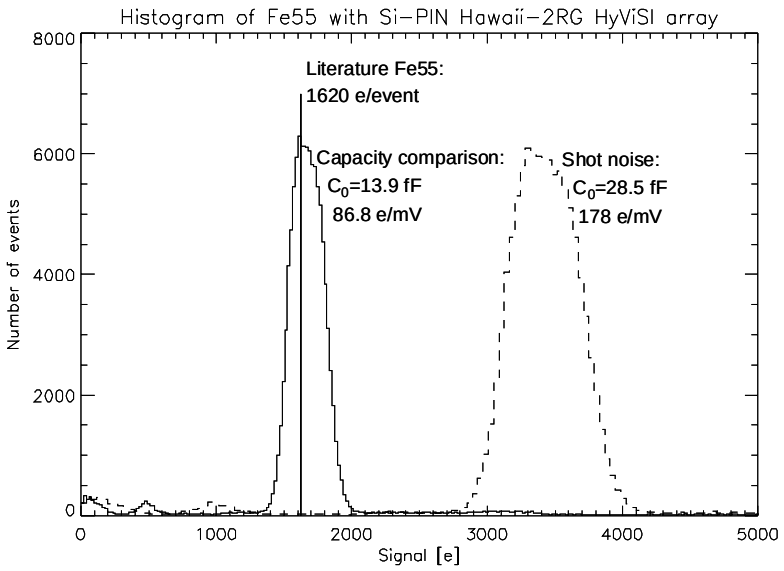

Figure 5. Histogram of Hawaii-2RG Si-PIN HyViSI array exposed to Fe55 X-ray source. The same data set is plotted with nodal capacitances derived from capacitance comparison method (solid histogram) and the shot noise method (dashed histogram). Literature value is indicated as a vertical line.

3. INTERPIXEL CAPACITANCE

The nodal capacitance C_0 derived by the shot noise method appears to be too large. Since Eq. (1) shows that C_0 is inversely proportional to the variance, the measured variance of the detector signal $\langle V^2 \rangle$ should be larger to obtain a smaller but more plausible nodal capacitance. The discrepancy cannot be explained by excess noise of the data acquisition chain as more noise would only make the variance larger not smaller. On the contrary, a mechanism has to be introduced which does not store signal charge but reduces the photon shot noise of a single pixel. The larger capacitance seen by the shot noise may be explained by coupling capacitance between neighboring pixels. As a consequence of the interpixel capacitance the signal of a pixel is spread by capacitive coupling to adjacent pixels, which reduces the apparent photon shot noise. The photon shot noise method does not yield the pixel capacitance C_0, but the provides a measure of the sum of C_0 and

all the coupling capacitors in series with the nodal capacitors of the neighboring pixels as shown in Figure 7.

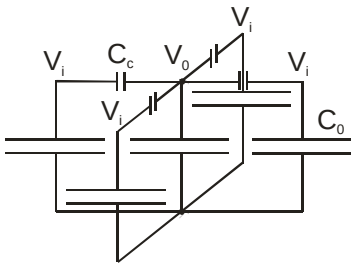

Figure 6. Interpixel coupling capacitance

Using the coupling capacitance C_c and the ratio of coupling capacitance and nodal capacitance $x = C_c/C_0$, a simple model of the apparent capacitance seen by the shot noise is $C = C_0(5x+1)/(x+1)$. For simplicity, only coupling to the 4 closest neighbors is considered here. By applying Kirchhoff's law it can also be shown, that the total signal with coupling V_0+4V_i is equal to the total signal V without coupling, i.e $V_0+4V_i = V$ with V being the signal for $C_c=0$. This implies that the interpixel capacitive coupling conserves photometry. For uniform illumination of the array no signal charge is stored on the coupling capacitors. The coupling capacitors reduce the photon shot noise because the voltage response of a photon-generated electron is not confined to a single pixel, but spread over all neighboring pixels. This nominal reduction of noise is accompanied by reduced image contrast and degraded detector MTF.

The effect of interpixel capacitance has been simulated numerically by generating random Poisson distributed short time exposures as shown in the upper halves of Figure 8 as surface plots, and in the upper halves of figure 9 as images. The right sides of Figures 8 and 9 represent a detector without interpixel coupling whereas the left sides of these figures introduce an interpixel capacitive coupling of x = 0.3. The crosstalk can be clearly seen in the upper left quarter of both the surface plot of figure 8 and the image of figure 9. The lower half of figure 8 and figure 9 show the images with and without interpixel coupling for a much longer integration time with a larger intensity scale.

The pixel to pixel variance without coupling on the right side is equal to the average number of integrated photons in agreement with Poisson statistics. The variance with capacitive interpixel coupling is smaller as shown by the smoother surface and image in the lower left quadrants of figure 8 and 9. The ratio of the standard deviation with capacitive interpixel coupling σ_c and the standard deviation without coupling σ_0 as derived from the numerical simulation using Poison statistics is shown by diamonds in figure 10. For small coupling ratios C_c/C_0 , the ratio σ_c/σ_0 follows the ratio of the total capacitance C and the nodal capacitance C_0 which is represented by the solid line in figure 10. This ratio is given by the expression $C/C_0=(5x+1)/(x+1)$ taking into account only the coupling to the four closest neighbors.

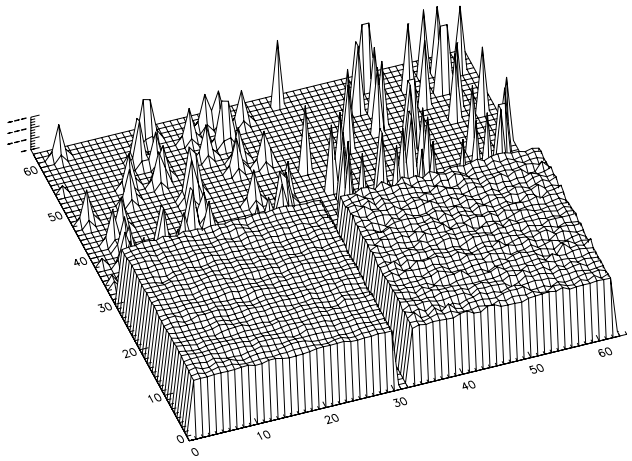

Figure 7. Surface plot of numerical simulation illustrating effect of interpixel capacitance. In this example, the interpixel capacitance is made relatively large, x = 0.3, to dramatically demonstrate the effect. Upper half short time exposure showing signal of individual, Poisson distributed photons. Lower half: long time integration with reduced intensity scale. Right half: no interpixel capacitance. Left half: With interpixel capacitance, signal of single photon is spread to closest neighbors. Long exposures show a smoother surface.

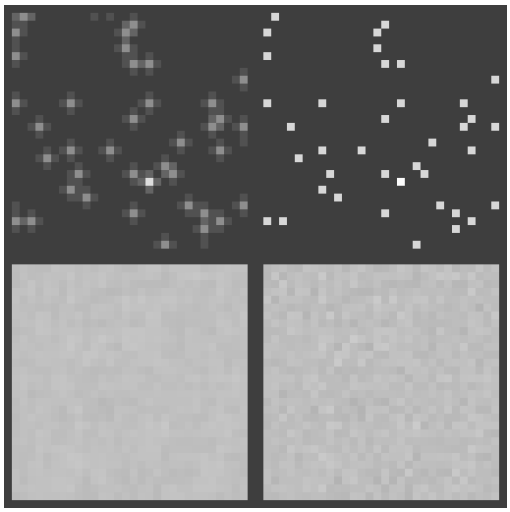

Figure 8. Image of numerical simulation illustrating effect of interpixel capacitance as explained in figure 8.

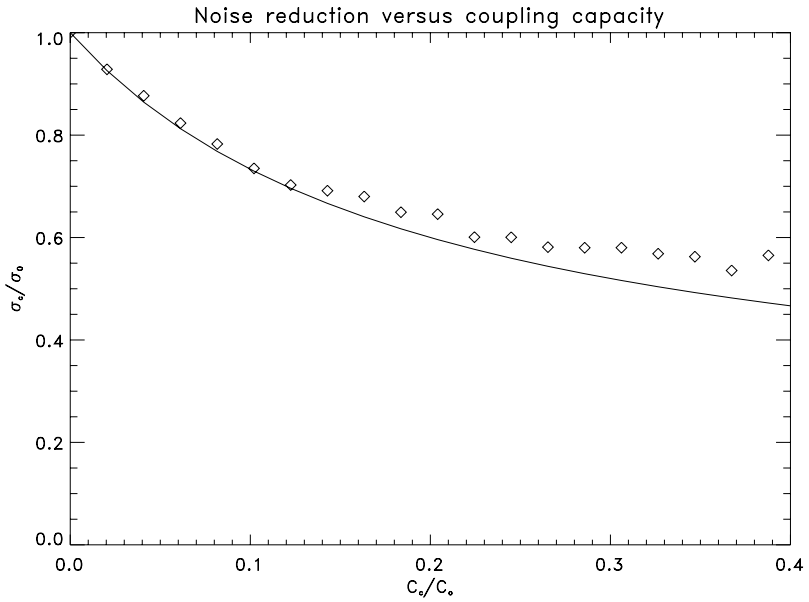

Figure 9. Ratio of standard deviation with interpixel capacitive coupling σ_c and without interpixel capacitive coupling σ_0 as function of coupling C_c/C_0. Diamonds: simulation of random Poisson distributed short time exposures. Solid line: ratio of total capacitance C and nodal capacitance C_0 taking into account the four closest neighbors $C/C_0=(5x+1)/(x+1)$.

4. AUTOCORRELATION

A. Moore et al.[2] have examined the detector edge spread and MTF; they were the first to introduce interpixel coupling as one mechanism to degrade the image sharpness of CMOS hybrid detectors. They devised a stochastic method of measuring the interpixel coupling using 2D autocorrelation and arrived at the same conclusion regarding the overestimation of the nodal capacitance by the shot noise method. We have applied their autocorrelation method to both HgCdTe and Si-PIN diode arrays hybridized to the Hawaii-2RG multiplexer. If the difference of two uniformly illuminated shot noise limited images have pixel intensities $V_{i,j}$, and $R_{m,n}$ is the autocorrelation function, the factor φ by which the nodal capacitance is overestimated by the shot noise method using "noise squared versus signal", is given in Eq. (3)

$$\varphi = \sum_{m,n} R_{m,n} \qquad with \qquad R_{m,n} = \frac{\sum_{i,j} V_{i,j} V_{i+m,j+n}}{\sum_{i,j} V^2{}_{i,j}} \tag{3}$$

If all the cross products $V_{i,j}V_{i+m,j+n}$ with $m \neq 0$ and $n \neq 0$ are 0, the signals of neighboring pixels are not correlated, since the interpixel capacitance is negligible. For this case φ is 1 and the "noise squared versus signal" method yields the correct nodal capacitance. If there is a correlation between neighboring pixels due to coupling capacitances, the correct nodal capacitance can still be derived from the shot noise of difference images by properly taking the correlation between pixels into account which is expressed by the correction factor φ given in Eq. (3).

We determined the correction factors φ for the nodal capacitance of CMOS hybrids with the 2D autocorrelation method of A. Moore. The measured values are φ_{HgCdTe}=1.20 for the HgCdTe array and $\varphi_{Si\text{-}PIN}$=2.03 for the HyViSI Si-PIN array. Both arrays are hybridized to the same type of Hawaii-2RG multiplexers. The correction factors are in good agreement with the results given in table 1 and further support the results obtained with the capacitance comparison method described in this paper.

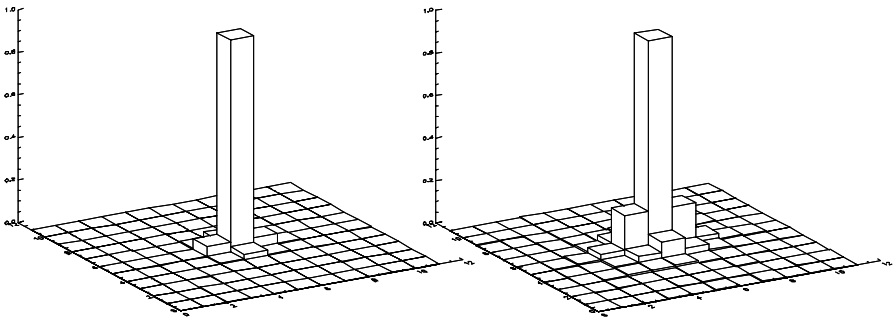

Figure 10. Autocorrelation of CMOS Hawaii-2RG hybrid arrays. Left: λ_c=2.5 μm HgCdTe array, φ=1.23. Right: Si-PIN HyViSI array, φ=2.03.

5. CONCLUSIONS

Modern CMOS hybrid focal plane arrays have small pixels. Hence, the coupling capacitances between neighboring pixels, even if they are only a few percent of the nodal capacitance of the detector pixel, have to be taken into account when the conversion gain is determined with stochastic methods. The usual "noise squared versus signal" method can lead to an overestimation of the nodal capacitance of more than 20% for infrared arrays and more than 100% for Si-PIN diode arrays. An alternative method of measuring the nodal capacitance, the capacitance comparison technique, is the most direct method which is also simple to implement. It delivers nodal capacitances which yield plausible quantum efficiencies well below 100%. Furthermore, it is consistent with the 1620 electrons generated in silicon PIN diodes by the absorption of K_α x-ray photons emitted by Fe^{55}. Additional confirmation for the capacitance comparison method comes from a stochastic method based on 2D autocorrelation to determine the nodal capacitance.

The high spatial resolution of extremely large telescopes will require focal planes of several Gigapixels. This future demand entices detector manufactures to increase the detector format by shrinking the pixel size, because available detector substrates are limited in size. This trend should not be followed, however, without carefully addressing all issues of interpixel coupling. For smaller pixel sizes, designs and techniques have to be developed to minimize the capacitive coupling between neighboring pixels. The spacing between indium bumps can be increased by using

smaller indium bumps. Epoxy glues with high dielectric constants between the indium bumps should be avoided, if possible, however for substrate removal, epoxy "backfill" may be necessary. Investigation into designs and fabrication techniques to reduce interpixel capacitance has already commenced at the Rockwell Scientific Company.

The authors received data from the VISTA[4] project which has infrared hybrid arrays with slightly larger pixel sizes of 20 μm. The arrays have no epoxy backfill between the indium bumps. Data have been analyzed with the 2D autocorrelation method. A correction factor of φ=1.03 has been calculated, a result reported independently by M^{c}Murty et al[5].

The Si-PIN diode array is hybridized to the same Hawaii-2RG multiplexer as the HgCdTe infrared array, but has much larger interpixel coupling capacitances. In this case, the main contribution to the interpixel capacitance is not located in the multiplexer or between the indium bumps, but in the Si-PIN diode arrays itself. It will be a challenge to substantially reduce this coupling.

Capacitive coupling between detector pixels is a deterministic process which conserves photometry and can be accounted for, if properly calibrated. In the photon noise limited regime both the signal and the noise are attenuated by the same factor. However, for point sources in the read noise limited regime the spreading of the signal response to neighboring pixels seriously affects the signal to noise ratio and degrades the detector MTF and image sharpness. This will degrade the performance of high order adaptive optics systems. For these reasons the advantages and disadvantages of reducing the pixel size to provide larger detector formats have to be carefully weighed.

6. ACKNOWLEDGEMENTS

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