SIDECAR ASIC @ ESO

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ABSTRACT

Teledyne Imaging Sensors (TIS) has developed a CMOS device known as the SIDECAR application-specific integrated circuit (ASIC). This single chip provides all the functionality of FPA drive electronics to operate visible and infrared imaging detectors with a fully digital interface. A Teledyne 2K×2K silicon PIN diode array hybridized to a Hawaii-2RG multiplexer, the Hybrid Visible Silicon Imager (HyViSI) was read out with the ESO standard IR detector controller IRACE, which delivers detector limited performance. We have tested the H2RG HyViSI detector with the TIS SIDECAR ASIC in 32 channel readout mode at cryogenic temperatures. The SIDECAR has been evaluated down to 105 Kelvin operating temperature and performance results have been compared to those obtained with external electronics. Furthermore ESO has developed its own interface card to replace the JADE USB card provided by Teledyne. The ASIC controller is now being embedded in the ESO standard VLT hard and software environment. This paper provides an update on the recent development of the new ESO ASIC interface card. We find that the SIDECAR ASIC provides performance equal to external electronics.

Keywords: ASIC, SIDECAR, Conversion gain, interpixel capacitance, CMOS hybrid, quantum efficiency, Hawaii-2RG, Si-PIN, HyViSI, IR detectors, HgCdTe

1. INTRODUCTION

At ESO and in most astronomical applications external control electronics is used to control detectors in the visible and infrared wavelength range. The recent controllers used at ESO have been FIERA and IRACE which are planned to be replaced by a new design called the New General Detector Controller (NGC) [Meyer et. al. 2005 and 2009]. Teledyne Imaging Sensors offers an alternative to discrete external electronics, the SIDECAR ASIC. This Application-Specific Integrated Circuit (ASIC) includes all capabilities to operate focal plane arrays on a single chip. This ASIC will be used to control detectors on the James Webb Space telescope and has been used to repair the ACS camera on the Hubble Space Telescope, reading out CCD devices. ESO has purchased the SIDECAR ASIC for test purposes and built a test system reading a Teledyne Hawaii-2RG detector to demonstrate the SIDECAR's performance for ground-based astronomy. The detector we have tested with the ASIC is a Teledyne 2K×2K silicon PIN diode array hybridized to a Hawaii-2RG multiplexer, the Hybrid Visible Silicon Imager (HyViSI). The detector is an optical sensor, analogous to near-infrared (NIR) array detectors. The separation of photon collection from readout facilitates separate optimization of the readout integrated circuit (ROIC) and the detector array. The main difference to IR detectors is that for silicon PIN the full bulk of the detector material is depleted whereas IR detectors are depleted only in the region of the p-n junction. Note that a hybrid differs substantially from a monolithic CMOS imager. In a monolithic CMOS imager, both readout and photon detection take place in the same piece of silicon. As nearly the full bulk of the detector is in depletion, silicon PIN detectors have good QE at both red and blue wavelengths. This Silicon PIN detector is operated at a high bias voltage (~10 Volt) compared to near-IR detectors. This detector has been extensively tested in 2006 (Dorn et. al., 2006) in 32 channel mode with the ESO external detector controller IRACE, and its performance is now being compared to the results obtained with the SIDECAR ASIC. The use of this kind of optical detector also simplified strongly the cryostat design and the turnaround time for warming up and cooling down cycles, as the detector and ASIC only needed to be cooled to ~105 Kelvin for optimum performance.

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2. SIDECAR ASIC ARCHITECTURE

The SIDECAR ASIC is a fully programmable control and digitization system for analog image sensors. It operates from room temperature to cryogenic temperatures as low as 30 K. Figure 1 shows a block diagram of a typical ASIC detector system. The top block represents the detector, which is connected to the ASIC via analog and digital lines. At the bottom of the ASIC block, only digital connections go to the external data acquisition system. Due to the immunity of the digital signal transmission which can be LVDS or CMOS, the back end system can be located several meters from the ASIC. The basic SIDECAR architecture, as shown in the diagram, can be divided into the following major blocks: analog bias generator, A/D converter, digital control and timing generation, data memory and processing, and digital data interface [Loose et al. 2003].

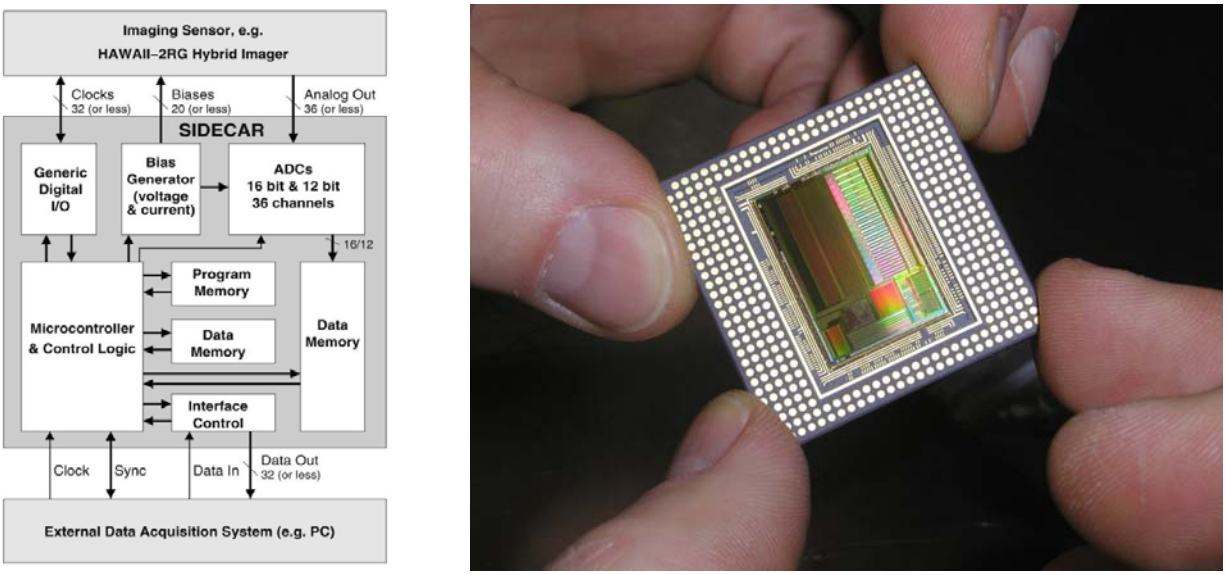

Figure 1 Block Diagram of the SIDECAR ASIC (Picture credit M. Loose) and ASIC in a 337-pin µPGA package (ESO)

The analog bias generator consists of 20 independent channels, each of which is composed of a 10-bit digital-to-analog converter and an output buffer with adjustable driver strength. Each channel can be used as a programmable current and voltage source. For reading out the analog detector signals, the ASIC provides 36 analog input channels. Each analog input channel can be digitized by on-chip ADCs offering 16-bit resolution at sample rates up to 500 kHz and 12-bit resolution at sample rates up to 10 MHz. A fully programmable and application optimized microcontroller provides ASIC control and generates the timing patterns of the image sensor clocks. A total of 32 digital I/O channels can be individually adjusted for driver strength and signal direction. Additional on-chip memory permits simple data processing functions such as pixel averaging or data sorting. Finally, serial and parallel data interfaces are implemented to read the digitized pixel values and to program the ASIC. Figure 1 shows the ASIC in a 337-pin LGA package used at ESO. The dimensions of the ASIC die are 22mm by 14.5mm. About two-thirds of the SIDECAR area is used by the 36 mixed-signal data channels consisting of preamplifier, ADC, array processor and data memory. A summary of the most important ASIC properties is given below.

Focal Plane Control and Read-Out Capability:

- 36 analog input channels
- Up to 500 kHz A/D conversion with 16 bit resolution per channel
- Up to 10 MHz A/D conversion with 12 bit resolution per channel
- Preamp gain = 0dB …27 dB in steps of 3dB
- 32 programmable digital I/O (clock generation)
- 20 programmable bias voltages/currents
- 16 bit microcontroller
- Efficient power-down modes
- 1-24 parallel digital output channels for data transfer (LVDS or CMOS)

Reduced System Space, Weight and Power:

- < 100 mW at 100 kHz 32 – channel operation
- Chip dimensions ~ 22mm x 15 mm using deep submicron CMOS processing
- Only requires one power supply, one fixed reference and one master clock for operation

3. SIDECAR ASIC SETUPS AT ESO

3.1 Warm setup with development board

To demonstrate the performance of the SIDECAR ASIC we initially started with a warm development kit consisting of the JADE2 card (the USB2 interface card between the ASIC and the PC), a warm development board and a Hawaii-2RG bare multiplexer to develop the microcode to readout the detector with 32 channels. A picture of this setup is shown in Figure 2.

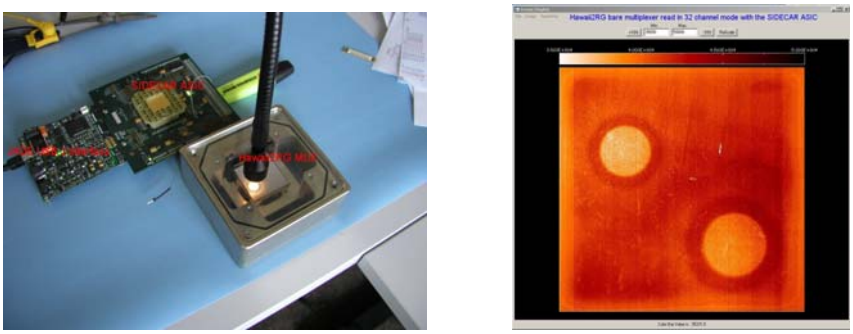

Figure 2 Initial setup of the SIDECAR ASIC on a development board reading a Hawaii-2RG bare multiplexer in 32 channel mode at room temperature

Different readout configurations have been tested using single ended and differential mode (with the reference pixel connected) and also the behavior of the ASIC during idle and exposure modes has been studied. A file of assembly code contains the pre-assembled program to perform acquisition of a H2RG. To download the SIDECAR ASIC firmware, the file must be assembled to derive a file in machine code description. This format contains all the necessary load directives and machine code that comprises the firmware. The firmware can be downloaded via the Interactive Development Environment (IDE) interface which comes with the software package. Upon downloading the firmware the SIDECAR ASIC begins to run the H2RG acquisition program. The very first program sequence is to initialize the memory and program the SCA via the SIDECAR ASIC SPI block. At this point the program remains in one of the two pre-configured Idle or Exposure states and can be controlled by writing dedicated registers. Programmable exposure parameters allow to obtain read, reset and drop fames as illustrated in Figure 3.

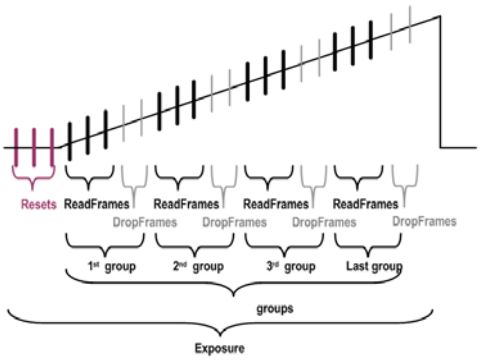

Figure 3 Illustration of a ramp as a function of the programmable Exposure parameters

3.2 Cryogenic setup with visible Hybrid detector

The Cryogenic-Development Kit consists of a SIDECAR ASIC packaged in a 337-pin LGA ceramic package, the SIDECAR ASIC Cryogenic-board, a 15" Flex Cable connects the SIDECAR ASIC Cryogenic-board to the JADE2 card or in our case the ESO NGC2ASIC interface. The JADE2 card is the interface between ASIC and PC running Windows and can also be attached to the cryostat on the outside. We have implemented the components in a CCD cryostat cooled by an ESO continuous flow cryostat allowing us to cool the HyViSI detector and ASIC to around 100 Kelvin with LN2. Figure 4 shows the setup inside the detector head, the cooling braids and flex cable configuration.

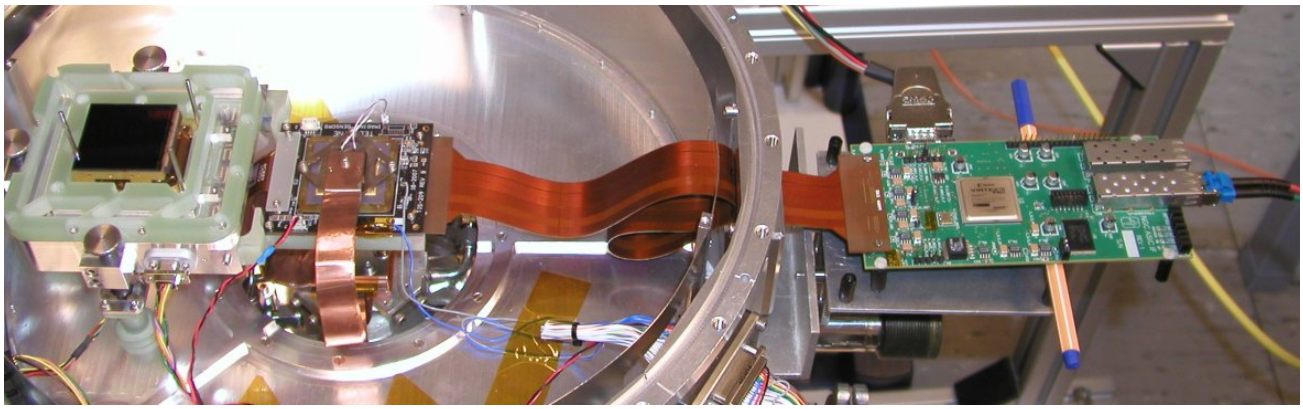

Figure 4 Cryogenic setup with ASIC and HyViSI FPA in the ESO test cryostat.

3.3 Initial setup modifications

In the default configuration using the JADE2 card connected to the USB2 port of a laptop or PC and the standard JADE2 jumper configuration the image shows some very strong pickup noise over a broad band of frequencies. Especially some low frequencies produce a strong pattern as seen in Figure 5 (left). We investigated a couple of options to reduce this pickup. The most effective modifications are to supply the analog 5V power to the JADE2 card with a clean voltage from a linear power supply and to electrically insulate the USB connection with a fiber link to the PC. Also the USB converter should be operated with a linear power supply to reduce pickup noise. Finally some improvement can be seen by grounding the ASIC backplane (substrate) to analog ground on the ASIC cryogenic board. Fine-tuning of the operating voltages (for both the detector and the internal voltages for the preamp) and some microcode optimization lead to a performance of 2.7 electrons readout noise, leaving a very clean image as shown in Figure 5 (right).

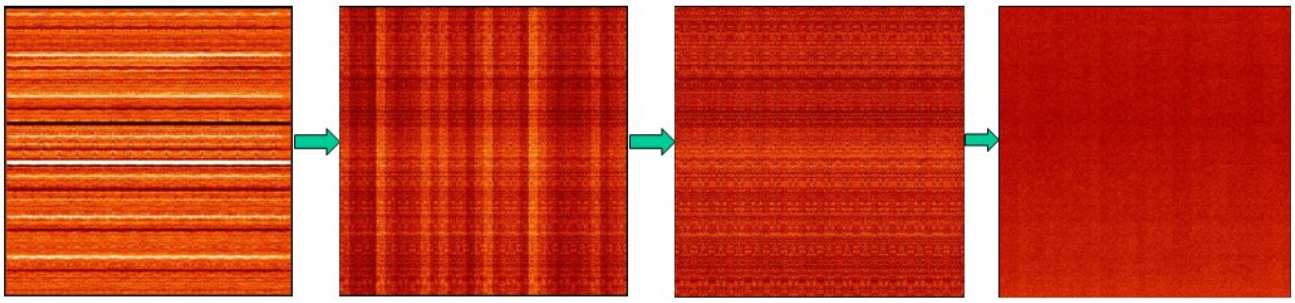

Figure 5 Various DCS images during optimization of the ASIC and HyViSI array for low noise operation (see text above)

4. CONVERSION FACTOR

4.1 FE-55 measurements and conversion factor

Usually the nodal capacitance C_0 of a detector pixel can be calculated from the slope of a plot of noise squared signal versus mean signal, the photon transfer curve [Janesick]. However, this method only works if the signals of neighboring pixels are uncorrelated. Current HyViSI detectors suffer from interpixel coupling which smooths the image and attenuates Poisson noise, introducing an error of up to 50 % for the conversion factor measured with the signal versus

noise method. In the past, this led to wrong values by determining the QE of the detector by almost 100% [Dorn, 2006]. Hence, we measure the conversion factor for the HyViSI read by the ASIC with an Fe-55 X-ray source. To perform the test with the HyViSI detector, a plexiglas window with a thickness of 2 mm was used not to attenuate the X-rays too much to allow enough events on the detector. An Fe-55 source with 1 MBq was used and installed on a special window (see Figure 6). Moreover to obtain the nodal capacitance C_0 by a direct measurement which does not rely on statistical methods, a simple but very powerful technique has been developed. It is based on comparing the voltage change of a large calibrated external capacitor to that of the unknown nodal capacitance C_0 which is many orders of magnitudes smaller [Finger et al., 2005]. For the HyViSI detector a nodal capacitance 13.9 fF was measured [Dorn, 2006]. The discrepancy of nodal capacitances C_0 determined by the capacitance comparison and the shot noise method are substantial and about a factor of two for the HyViSI detector. Thus, plausible quantum efficiencies cannot be achieved using the conversion gain derived from the shot noise method with the usual "noise squared versus signal" technique. The capacitance comparison method confirms the values measured with the Fe-55 measurements and leads to the conclusion that the shot noise method is wrong for this device. The Quantum efficiency has been measured at temperatures ranging from 120 to 200 K in steps of 20 K to reveal its temperature dependence [Dorn et. al., 2006]. The QE results fit very well with a modeled curve by Teledyne.

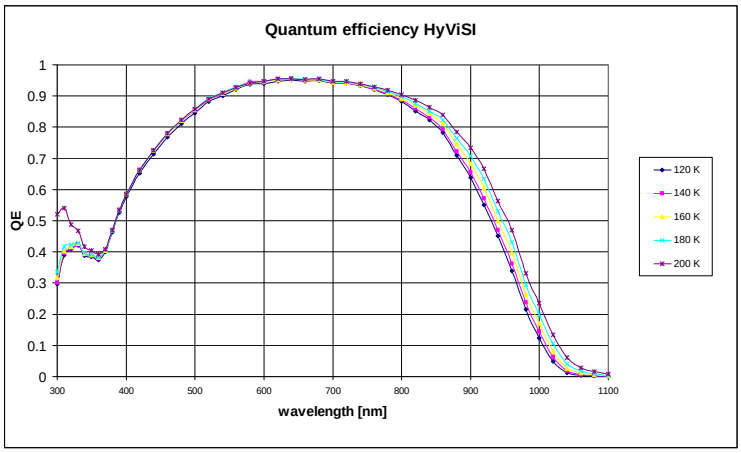

Figure 6 HyViSI QE at various temperatures

The events have been analyzed with a photometric routine and a histogram has been plotted (see Figure 7). A conversion factor of ~1.47 electrons/ADU was determined from the histogram for a gain setting of 9dB for the ASIC preamplifier.

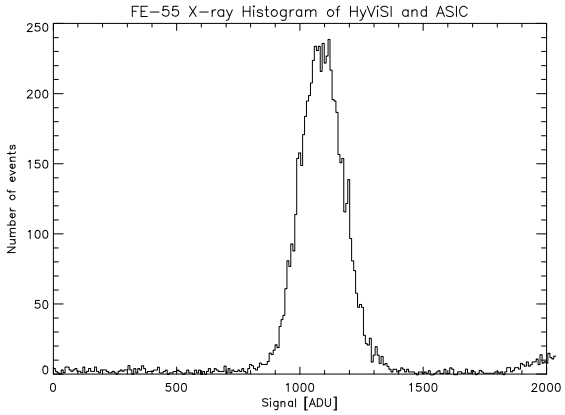

Figure 7 HyViSI FE-55 histogram leading to a conversion factor of 1.47 electrons/ADU

4.2 Conversion factor (calculation)

The ASIC contains an amplifier that provides gain to the analog signal before digitization. The pre-amp is capable of gains between -3dB to 27dB gain in 3dB steps. I.e. a gain setting of 9db corresponds to an electrical gain of 2.83. To verify that the values from the Fe-55 measurements are consistent, the conversion gain for different gains was calculated based on the nodal capacity measurement. For an electronic gain of the preamp of 2.83 and a nodal capacitance of 13.9 fF the conversion factor is:

$$c = \frac{s \cdot G}{g} = 1.53 \frac{e}{ADU} \qquad \text{with} \qquad G = \frac{C_0}{q} \qquad (1)$$

where:

c is the conversion factor in electrons/ADU , s is ADC sensitivity $3.3V/2^{16} = 50 \times 10^{-6}$ Volt/ADU,
g is electronic gain of the preamp, G is conversion gain in electrons/Volt and q is the electron charge.

This is consistent with a conversion factor 1.47 electrons/ADU derived from the HyViSI Fe-55 histogram. This calculation has been done for several gain levels and has been confirmed with Fe-55 measurements.

5. READOUT OPTIMIZATION

Channel offset compensation by using reference pixels:

Due to kTC noise or bias drifts at the input of the ASIC preamp, the 32 channels show a slightly different offset level in a difference image. This can be compensated by subtracting the mean of the embedded reference pixels on the top or bottom of the corresponding active pixels per channel. These reference pixels track those changes and can be used to compensate this offset. Figure 11 shows the result of this offline data reduction. The H2RG array of 2048×2048 pixels contains 8 rows and 8 columns of reference pixels arranged in blocks of 4 rows/columns around the border of the array. The reference pixels are rows 0 – 3 and 2044 – 2047 as well as columns 0 – 3 and 2044 – 2047. Rows and columns 4 – 2043 are all active pixels. Since these reference pixels are included in the main array, reference pixel readout is embedded in the normal image. To compensate the kTC noise the lower 4 pixels 0 to 4 were used to calculate the mean of the pixels and to subtract this value from the active pixel values. This needs to be done on a channel by channel basis. Note that this does not add any noise but a slight offset to the pixel values.

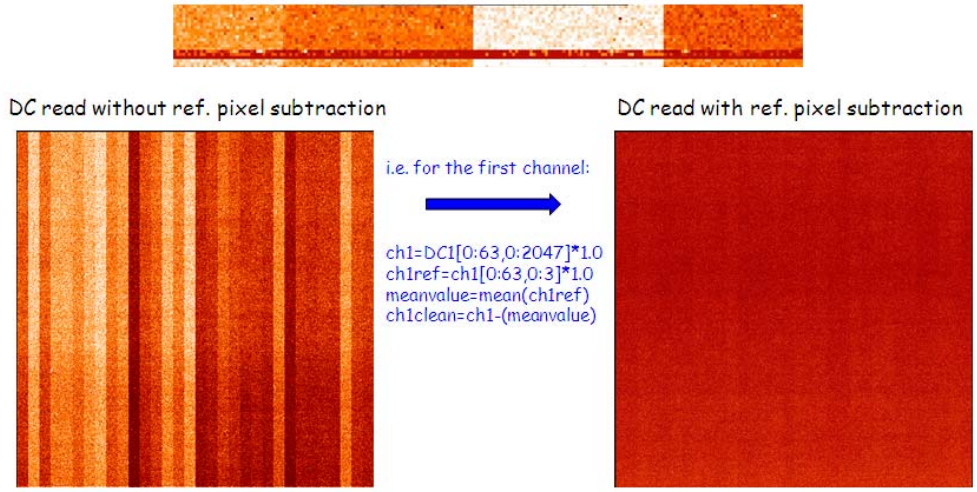

Figure 8 Offset compensation by subtracting mean value of the reference pixels on a channel by channel basis

6. READOUT NOISE

We have measured the current noise performance at different gain settings and compared those with the results obtained with the external electronics IRACE. Figure 15 shows a plot of read noise versus Fowler pairs with the detector operating at 105 Kelvin and the ASIC at 115 Kelvin. For as normal CDS read we obtain 7 to 9 electrons with the current configurations and can improve to as low as 2.7 electrons for 30 Fowler pairs (60 samples). The effect of conversion noise of the ASIC ADCs at lower gain can be seen in Figure 15. This noise quickly averages out after 3 Fowler pairs obtaining the same noise values as with a higher gain setting. With IRACE we have measured around 6 electrons for a DCS read and 2 electrons for 30 Fowler pairs. This noise with IRACE has been measured with a temporal method and hence cannot be directly compared to the measurements done with the ASIC. With the ASIC, the noise has been calculated from single images. The SIDECAR ASIC noise results are comparable to those obtained with the ESO IRACE external electronics.

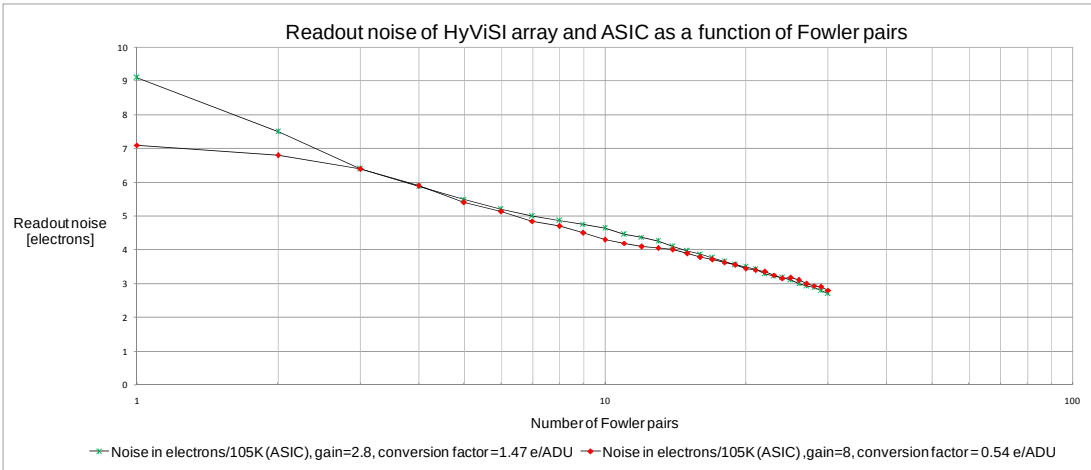

Figure 9 Read noise as a function of Fowler pairs for two different gain settings

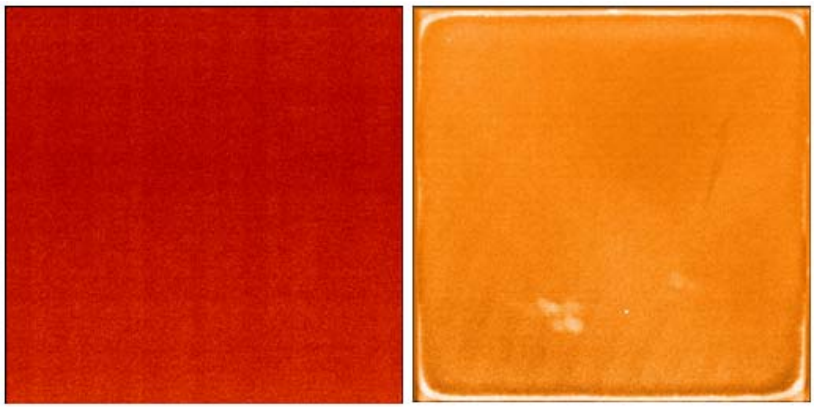

Figure 10 Comparison of images obtained with the SIDECAR ASIC and IRACE. The right image shows a single correlated double sample (CDS) obtained with the ASIC and the right picture the corresponding image obtained with the ESO external controller, IRACE.

Figure 10 shows a comparison of CDS images obtained with the SIDECAR ASIC (left image) and ESO's external controller IRACE (right image). The image obtained with the SIDECAR ASIC is clean and uniform and does not show the frame pattern apparent in the image taken with IRACE. This frame pattern depends on the time interval between the reset and the first read and can also be eliminated using the IRACE electronics by introducing a delay between the reset and the first read. Anyway, the pattern is not visible in a difference image taken with IRACE and therefore is not an operational issue.

7. DISCUSSION OF NOISE RESULTS

The shot noise method leads to different and wrong values because the detector pixels of the HyViSI suffer from capacitive coupling to its neighboring pixels. This interpixel capacitance smoothes the Poisson noise, causing it to appear to be smaller and hence the conversion factor to be larger. The responsive quantum efficiency is overestimated as the device appears to sense more photons than actually arrive on the pixel. Note that capacitive coupling is deterministic and should not be confused with the effect of charge diffusion. The conversion gain measured for HyViSI using Iron-55 x-rays and the capacitance comparison measurement method both determine the total conversion gain and need to be applied for QE measurements. For the QE the entire array is uniformly illuminated and thus the amount of "gain" lost from a node with charge to neighboring pixels is received back from the neighboring pixels since all are at the same light level. For the readout noise this conversion factor can only be used partly. Since we are measuring and calculating the readout noise of a single node, the total conversion factor in e/ADU will be too low. However the conversion gain used for all measurements and results is the one measured with Fe-55 in this paper. The authors think that it is important to state the method the conversion gain has been measured for all parameters.

8. ESO INTERFACE CARD DEVELOPMENT

To interface the ASIC controller to the ESO standard hard and software environment, we have developed our own interface card for the ASIC, replacing the JADE USB card provided by Teledyne. This interface card connects the ASIC to the standard ESO New Generation Controller PCI card via a fiber connection [Meyer et al., 2009]. The ASIC can now be controlled by the NGC software providing the same user interface as the ESO standard external detector controller [Stegmeier et al., 2009]. The NGC Back-End PCI module provides a connection to a 64 Bit PCI bus and is based on a XILINX Virtex Pro FPGA. The slave IF is used for communication, the master IF is used for video data DMA transfers to PCI. Two Rocket IO transceivers (2.5 GBit each) are used for communication and data transfers. Other options to increase bandwidth are possible (one FPGA contains 8 transceivers, space limit for PCI card size might be four).
In the beginning we used a single LVDS line for the communication link between the ASIC and the NGC interface. This single LVDS line has a bandwidth of 50 MBit. This limited the minimum readout time of the Hawaii2RG array to 1.7 seconds. In a next step the VHDL code of the NGC interface has been changed and a revised board has been produced to make use of 16 parallel data lines thus increasing the bandwidth to ~ 800Mbit. This reduced the readout time of the Hawaii2RG to ~100 ms.

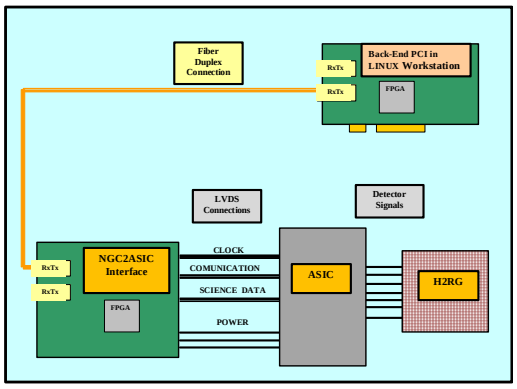

Figure 11 Blockdiagram of the ESO ASIC setup with the interface to the PCI card of the ESO standard controller electronics.

The user interface of the ASIC supports different digital interfaces but the NGC to ASIC interface uses the LVDS lines with serial protocol to program the ASIC registers and read the science data. The two main operations are:
ASIC Command IO: ASIC Communication Read or Write Operations are on LVDS serial links. They are used to set up the ASIC internal registers.
ASIC Science Read Operation: After the ASIC registers have been set-up and before the Start Read-out command is given to the ASIC, the science data capture has to be programmed in the Command Register Science Data Read. The ASIC then sends the digital data to the NGC2ASIC interface.

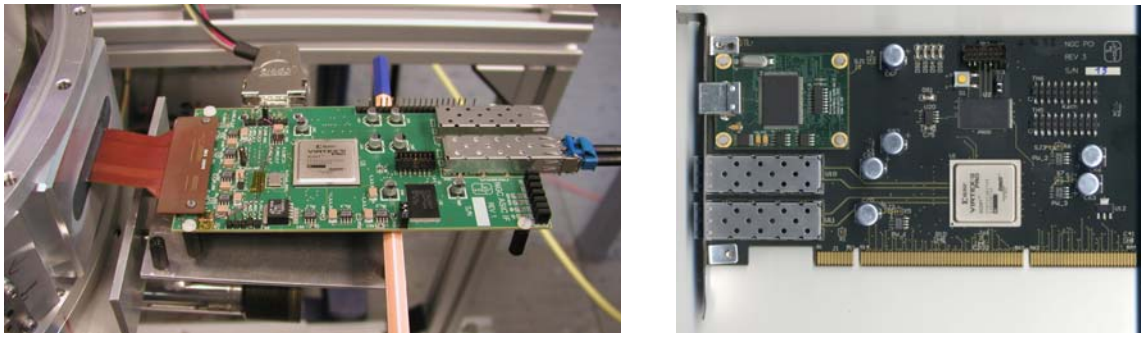

Figure 12 Pictures of the NGC backend PCI card (right) and the new ESO ASIC interface (left) connected via a fiber interface

With this interface we now can make use of the full functionality of the H2RG detectors using the ASIC/HxRG code (see below) provided by Teledyne. With the first revision we were limited to a single LVDs line but in 2010 a new revision of the card extended the functionality to 16 parallel data lines thus increasing the bandwidth to ~800Mbit. This will allow us to also test the fast output amplifiers of the H2RG detectors reading at a higher pixel frequency.

- Multiplexer type (H1RG, H2RG, or H4RG) and more
- Optical and IR HxRG detectors
- Number of detector outputs used (1,2,4,16,32)
- Number of SIDECAR ADCs averaged per output (1,2,4, 8)
- Cold or Warm operating temperature
- Pre-Amp gain, reset scheme, reference and current sourcing
- Buffered or Unbuffered mode on HxRG detector
- Horizontal clocking and pixel reset scheme (line by line, pixel by pixel, global)
- DC, Up the ramp or Fowler exposure settings (free to program)
- Window mode

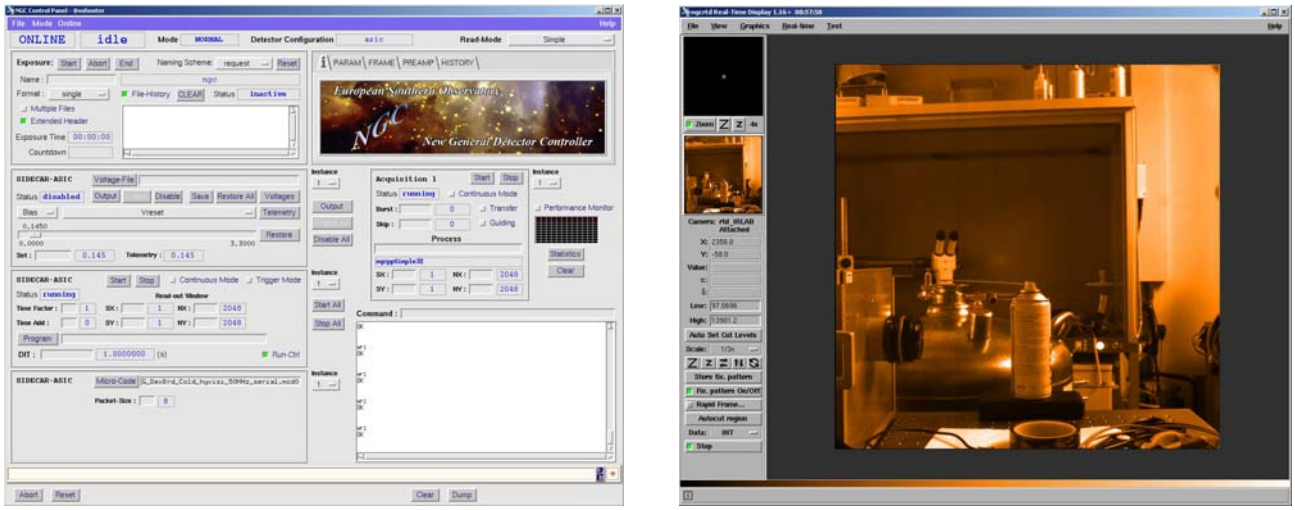

Figure 13 NGC graphical user interface and Real time display reading a H2RG HyViSI detector capturing an image in the lab

The full system needs less than 3 Watts and only one 5 Volts power supply. The weight of the ASIC systems (including the power supply) is less than 1 kg.

9. CONCLUSION

We have tested a SIDECAR ASIC in 32 channel mode with a Hybrid Visible Silicon Imager (HyViSI) from Teledyne Imaging Sensors reading at a pixel rate of 100 kHz. The detector is a complementary metal oxide semiconductor (CMOS) alternative to charge coupled devices (CCDs) for photons at optical wavelengths. The device suffers from interpixel capacitance which introduces an error in the determination of the nodal capacitance or conversion factor with the standard photon transfer method and hence the conversion gain was measured with a Fe-55 source. After initial setup problems we were able to obtain a noise performance with the SIDECAR ASIC of 7 electrons for a single CDS and as low as 2.7 electrons for 30 Fowler pair sampling. With the ESO standard IR detector controller IRACE we have measured noise levels of 6 electrons for single CDS (readtime ~1 sec) and as low as 1.8 electrons for 30 Fowler pairs (readtime ~25 sec). The SIDECAR ASIC readout electronics facilitates a great simplification to system design. Our next step will be testing the SIDECAR with a HAWAII-2RG IR detector with 2.5 micron cutoff wavelengths at 80 K operating temperature. We have furthermore developed our own interface for the SIDECAR ASIC (replacing the JADE2 card) and to include the SIDECAR in the standard VLT and E-ELT software environment.

10. ACKNOWLEDGMENTS

All tests have been performed in the ESO infrared detector lab. The author would like to thank Markus Loose, James Beletic, Raphael Ricardo and Richard Blank from Teledyne Imaging Sensors for their help getting the SIDECAR ASIC working in 32 channel mode and for many useful discussions.

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