Performance evaluation of 5 um cut-off Hawaii-2RG detectors using the fast readout amplifiers

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ABSTRACT

ESO has begun an ambitious mid-IR detector program with the funded development of a new Raytheon detector (AQUARIUS) and the further development of instruments to use 5 µm cut-off material Teledyne HAWAII-2RG detectors. Both these detector types are capable of extremely high readout speeds, through multiple readout ports, resulting in data rates in excess of 250 Mbytes/s. This has required further development of our new detector controller system (NGC) to allow it to operate at these very high pixel data rates. This has also entailed the development of new high speed pre-amplifiers which can operate at 60K to allow us to drive the long cable runs typical of an astronomical instrument. We report on the development and performance of our new higher speed NGC systems with particular regard to the operation of a Hawaii-2RG detector configured to use its high speed readout stages. We will present data on the performance of such at device, configured to operate in both slow and fast readout modes, with particular regard to noise versus pixel speed and also the optimization of the voltages.

Keywords: Hawaii-2RG, fast outputs, 5 µm cut off material, NGC, cryogenic pre-amplifiers

1. INTRODUCTION

Future ESO projects have requirements to run detectors at much higher pixel rates than is typical for astronomical instruments at present. These applications include adaptive optics and mid-IR applications. For example the ESO MATISSE [1] project requires operation of a H2RG 5 µm detector at pixel speeds greater than 1 MHz and operation of the AQUARIUS [2] mid-IR detector at pixel speeds in excess of 3 MHz. These high pixel speeds have many implications for the overall detector system design as part of a facility class astronomical instrument. The detector output impedance, cable capacitance, cable length and number of outputs have a great influence on the overall system design. Likewise the digitization electronics must be able to digitize at the required high speed and also be able to transfer the data for final processing and storage. The AQUARIUS detector system must operate at sustained data rates in excess of 250 Mpixels/second. This has meant continued development of our detector control system NGC, as well as the development of new high speed cryogenic pre-amplifiers. This paper gives a description of these new cryogenic pre-amplifiers as well as the system design of NGC which allows such high speed operation. We also present a detailed description of the work required to operate the HAWAII-2RG family of detectors using their high speed output circuitry, as well as some preliminary results from operation of these detectors at the higher pixel speeds. We also present dark current and other performance results specifically for our engineering grade 5 µm HAWAII-2RG detector.

2. THE NGC SYSTEM FOR HIGH SPEED OPERATION

2.1 NGC hardware

The NGC system has been described in depth elsewhere [3]. It is a modular and generic system designed to operate most detector types from large optical CCDs to high speed mid-IR detectors. There are two main groups of modules connected by a fiber duplex connection :

- The Detector Back-End Electronics (DBE), typically an in house designed PCI-X 66 MHz board.

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- The Detector Front-End Electronics (DFE) consisting of the Basic Module(s) and if needed additional acquisition (AQ) modules. These are interconnected by high speed copper serial links on a backplane for command and data transfer.

The basic link configuration is the linear connection of modules. Commands are routed always from the Back-End to the first Detector Front-End Electronics module. Additional DFE modules are addressed by wormhole routing from previous modules. The same happens for replies or video data from DFE modules to DBE modules. However the most important point for our applications is that if more communication bandwidth is needed as is the case for the high speed large detectors then video data can be routed directly out of the AQ modules to additional receivers, that is additional PCI based DBEs. This is clearly seen in Figure 1.
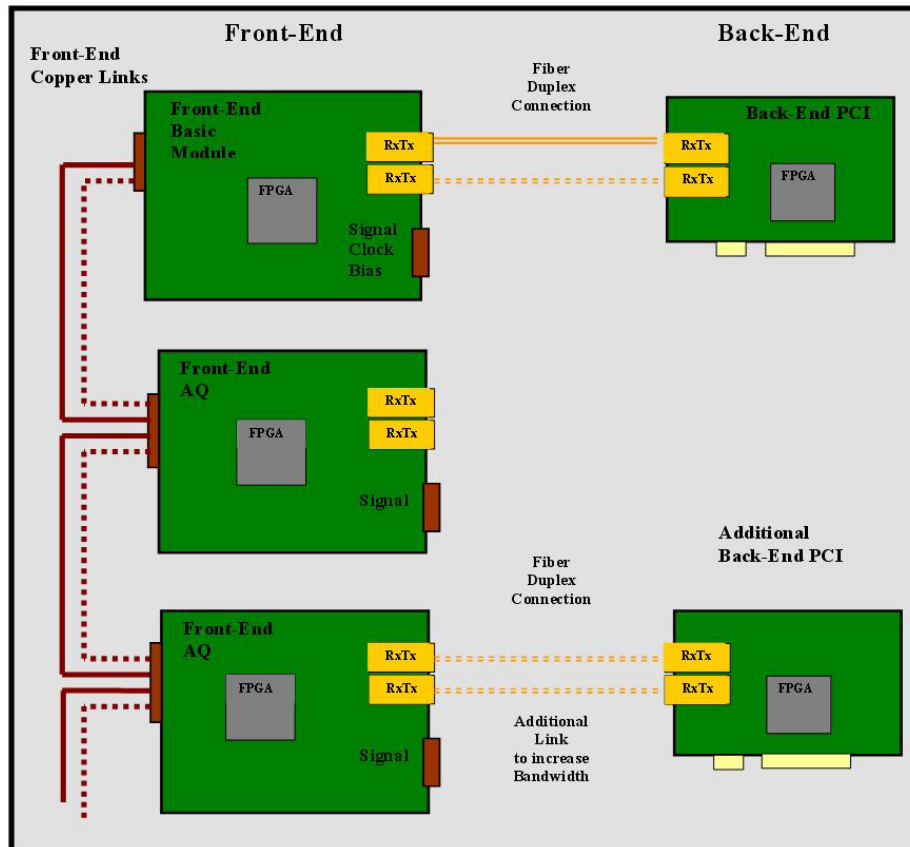

Figure 1: NGC system block diagram

2.2 NGC AQ Module

The NGC AQ module has 32 circuits used to digitise the 32 output channels from a typical IR detector. Each circuit is made up of a video chain consisting of a video buffer amplifier, set to a gain of one and the Analog-Digital Converter (ADC), all connected to an FPGA for control and onward transmission. The video amplifier is a fully differential design from input all the way through to the differential inputs of the ADC, and includes offset control and selectable bandwidth. Most importantly for our applications, different ADC types can be installed and used. The possible choice of ADCs are the AD7677, a 1 MHz/16 bit device, the AD7674 a 1 MHz/18 bit device and the AD7621 a 3 MHz/16 bit device. If more than 32 channels are required then additional AQ modules can easily be added and together with their individual fibre links means that the communication links on the NGC system itself do not become the bottleneck for any data transfer. A good example of this is the configuration used with the AQUARIUS detector which requires 64 video

channels operating at 3 MHz implying a date rate of 250 Mpixels/second. The bottleneck for this data rate is not NGC itself but rather will be the PC required to process this data and then store it. The latest generation of multi-core PCs, have up to 8 processors on board as well as multiple PCI buses and these will probably be capable of matching our pixel rate requirements. If not then a multi PC configuration will be used.

2.3 NGC FEB Module

The NGC FEB module communicates with the outside work. However it also contains the bias and clock generation circuitry necessary for operation of detectors. Up to twenty biases are available with individual level control using 12 bit DACs. There is also telemetry for all biases as well as over-voltage protection circuitry. The upper and lower clock levels are also user controllable. The standard waveform generator is 24 bits wide and can operate at speeds greater than 3 MHz.

3. CRYOGENIC PREAMPLIFICATION

3.1 ESO Standard Preamplifier

ESO have been using cryogenic pre-amplification circuits for many years. The standard circuit is shown in Figure 2 for clarity, together with the actual rigid-flexi implementation.
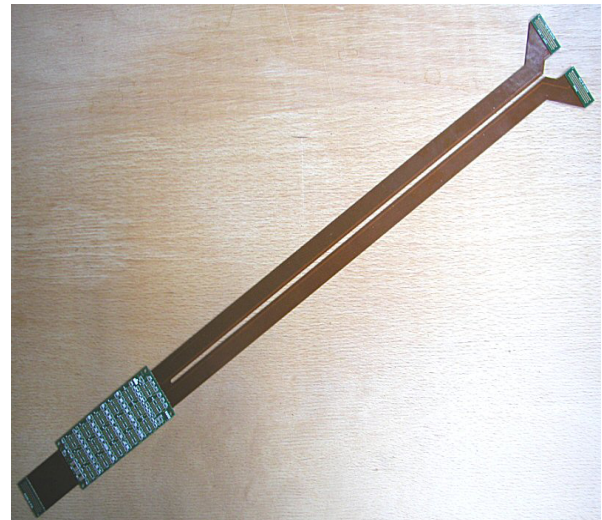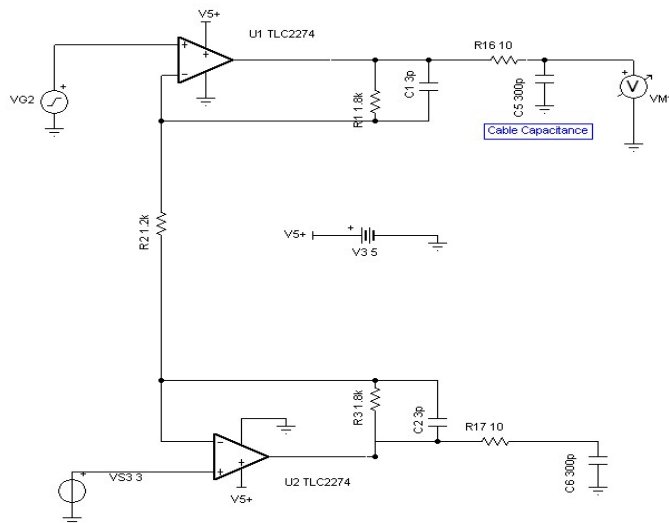

Figure 2: ESO cryogenic Preamplifier schematic left and PCB implementation right

The pre-amplifier is a fully differential design based on the TLC2274 CMOS op-amp. Four op-amps are available in each 14 pin package, allowing for two video channels per package. Seventeen such circuits are then repeated to allow implementation of all 32 channels in the Hawaii-2RG detector together with the windowed and reference outputs. This is a very mature design and has been in use for more than a decade in many ESO instruments. The circuit PCB is positioned within a few centimeters of the detector using two short flexi circuits. It then uses long, up to 1 metre in length, flexi rigid cable constructions to connect to the vacuum vessel wall and then via more standard 3 metre cable lengths to the NGC and digitization circuitry described earlier. All the flexi cables use a cross hatch copper pattern on top and bottom layers to give some level of shielding inside the cryostat. Being able to drive such long cables and the correspondingly high capacitance which would be seen by the detector output is only possible because of the use of these op-amps as well as the fact that the pixel speeds are relatively slow at 100 kpixels/second. The capacitance of the flexi circuits in use is particularly high and would be the limiting factor in any higher speed design.

3.2 New high speed cryogenic preamplifier

The preamplifier already described is an ideal match to a 100 kpixels/second rate, however it is close to the performance limit in terms of its gain-bandwidth product and could never be used with the faster read out stages of the HAWAII-2RG detectors. A newer design with faster op-amps was called for. If we assume that the maximum output swing of the detector is 1V, the maximum input voltage to the NGC digitization stage is 4V then an electronic gain of four is allowed. Likewise if we assume a maximum 3 MHz pixel rate, set by our 16 bit digitizers and a system bandwidth of 12 MHz then this implies that an op-amp with approximately 75V/µs slew rate and a gain bandwidth product of 50 MHz is required. The other important parameter is the noise performance of the op-amp. If we assume a detector with 15 e- rms read noise and a transimpedance conversion gain of 4 e/DN then for the noise bandwidth specified this implies that for the noise of the detector to be the dominant noise source then the noise of the op-amp should be less than 6 nV/√Hz. Finally the op-amp should preferably be CMOS rather bipolar to ensure good operability at cryogenic temperatures. This is because bipolar transistors rely on thermal excitation to allow for conduction and as such are subject to carrier freeze out as temperatures are lowered. Gain decreases as the temperature is reduced. CMOS can also suffer from freeze out but at lower temperatures. The gain of MOSFET devices actually improves as their temperature is reduced [4]. This is primarily due to the fact that the trans-conductance increases as a function of temperature due to the mobility increasing as temperature decreases. The threshold voltage may shift as a function of temperature but this does not impede the transistor gain, it may only change the operational point.

From this discussion we have derived a set of requirements for a pre-amplifier design with op-amps for cryogenic operation. Figure 3 below shows a table of possible op-amps which meets the requirements as well as doing a comparison against our original preamplifier design.

Manufacturer	Part Number	Slew Rate (V/us)	Unity Gain Bandwidth (MHz)	Noise (nV/√Hz)	Comment
Texas Instruments (T.I.)	TLC2274	3.6	2.2	9	4 per package, +/-8V
T.I.	OPA4354	150	250	6.5	4 per package, +5V
T.I.	OPA4350	22	38	5	4 per package, +5V
T.I.	OPA2356	360	450	5.8	2 per package, +5V
Analog Devices	ADA4891	170	240	10	2 per package, +5V

Figure 3: Comparison of op-amps for cryogenic operation

From the table we see that there is a reasonable selection of devices available from Texas Instruments which have much better performance parameters than the TLC2274 which is the device used in the standard ESO preamplifier. To ensure that these new devices would meet the requirements of a cryogenic preamplifier the circuit was modeled using TINA [5], an industry standard package for SPICE modeling. The results of this modeling are shown in Figure 4, together with a model for the standard preamplifier.

From the A.C. transfer characteristics (Bode plots) we can see the much improved gain bandwidth response of the OPA4354 op-amps compared to the TLC2274 devices. It is also intuitive to look at the phase response when the gain is zero. This gives a good indication of the stability of the circuit. Theoretically we are looking for less than 180 degrees of phase response for zero gain to ensure good stability, in fact we would want to be at 30 degrees less than this to give a good margin for stability. For our design this is indeed the case. The addition of input, output, or load capacitance to an op-amp circuit decreases stability and leads to overshoot in the time domain. Input capacitance is easily compensated by adding a feedback capacitor into the circuit. The input capacitance can also be minimized by removing the power plane around the inputs to the op-amps. The circuits have been modeled with the expected cable capacitances seen in the flexi boards. TINA is also very useful in modeling the expected noise performance for the required circuits at the operating frequencies.

However to ensure that the actual performance of the pre-amplifier circuit comes close to the modeled performance then good high frequency circuit design and PCB layout is also required to minimize stray capacitance. Op-amp data sheets are usually a good starting point for this but more important is to work with experienced PCB design and layout engineers.

The final pre-amplifier design should minimize capacitance at op-amp inputs as well as using impedance matched cabling at the outputs, including any flexi rigid PCBs. For our laboratory testing we have not done a new design but rather only modified the board already shown above. This board is not optimized for high speed design but is a useful starting point and allows easy performance comparison with the standard ESO setup.
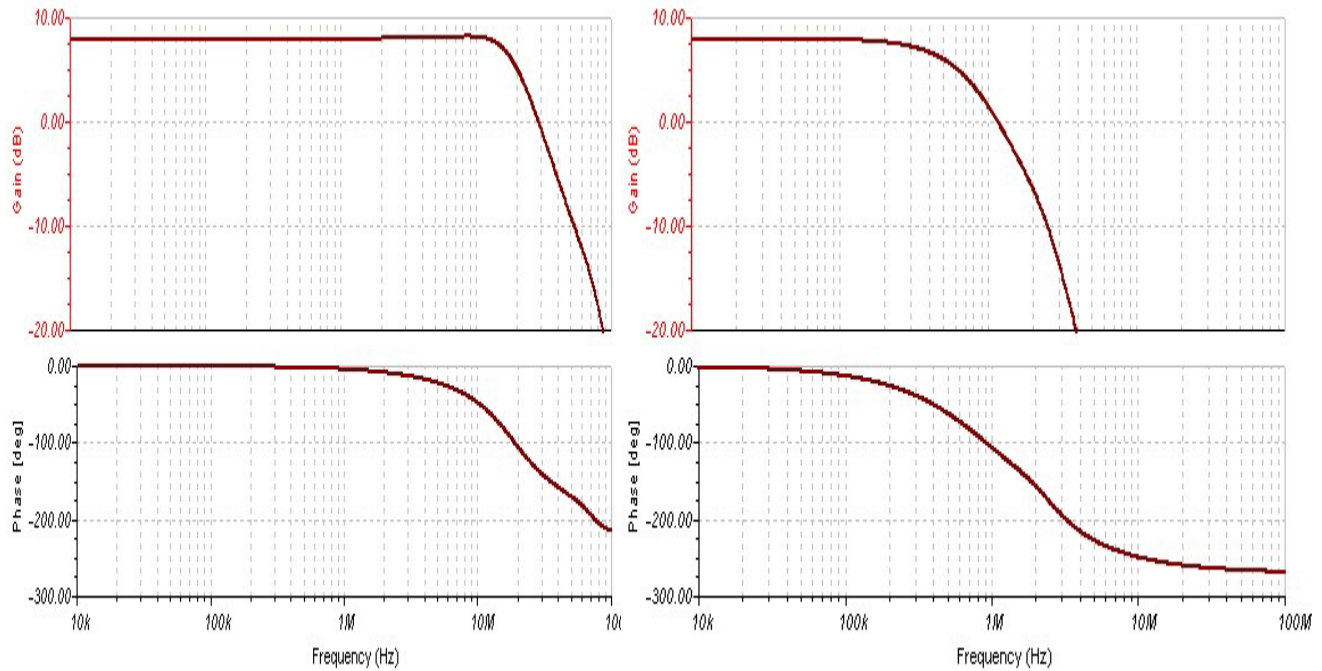

Figure 4: AC Transfer Characteristics for OPA4354 (left) and TLC2274 (right) op-amps. Top plot shows gain response and bottom plot shows phase response.

3.3 Cryogenic testing of preamplifiers

For evaluation purposes our preamplifier design was build onto a small PCB for mounting in a liquid nitrogen cryostat. The gain of the circuit was set to four and the devices were cooled to less than 90K. A commercial high speed waveform generator was then used to inject a square wave with controllable slew rates into the op-amp. A comparison was then made between input and output waveforms. The main areas for testing were that the gain and slew rate would be stable with temperature. The op-amps performed as expected all the way down to 90K. Our setup did not allow us to go colder than this. The supplies to the op-amps were also switched off and the op-amps were allowed to cool down to 90K. They were then switched off and on many times to ensure operation. It has been reported [6] by others that the OPA350 CMOS op-amps suffered from switch on effects when cold, but this has not been the case for our setup. This is probably because we use a control circuit to soft-start and soft-stop the supplies to the op-amps when they are switched on or off. The reason for using the soft start/stop circuit is that we also have a requirement to also use this preamplifier with the AQUARIUS detector. However the output of this detector has a d.c. level of 7V with the signal modulated downwards from this d.c. level by the order of 1V. This d.c. level is not matched to a CMOS op-amp circuit which runs from a single +5V supply. We have therefore allowed for our preamplifier design to be operated also from an upper +10V supply and lower +4V supply as well as the single 5V supply. The design must ensure that the op-amps are not damaged at switch on if, for example, the +10V supply were to be switched on before the +4V supply then we would have 10V across the supply rails of the devices which would potentially destroy them. We have therefore implemented a circuit which

switches both these supplies on at exactly the same time and in a linear manner. The final disadvantage of using the faster op-amps is their increased quiescent current compared to the TLC2274, in fact more than a factor of two larger at 5 mA per op-amp. Since there are sixty-four op-amps per pre-amplifier board then the current demands increase dramatically, the main issue being then the resistive voltage drop down the thin tracking of the copper flexi boards we use to connect from preamplifier to hermetic feed-through connectors. The resistance of the power tracking is substantial at 6 ohm which leads to an excessive voltage drop. For our laboratory experiments we have added parallel external cabling to the flexi PCBs to minimise this resistance.

4. HAWAII-2RG 5 MICRON PERFORMANCE

ESO have recently borrowed a 5 μm cut-off version of the HAWAII-2RG from Teledyne in anticipation of ordering a science grade device in the near future for the MATISSE project. This is a mid-infrared spectro-interferometer project combining up to four UTs/ATs beams of the VLTI. For our project the important parameters to be measured were the dark current and the performance of the detector at pixel rates greater than 1 MHz.

4.1 Dark current measurements

Figure 5 is a dark current plot for our engineering grade detector as tested in our laboratory facility. Our test setup photon background is approximately 30 electrons/pixel/second. Therefore we have had to "blind" the detector using a cold cover plate to be able to measure dark current rates when below 80K. The plot shows clearly that the detector dark current is diffusion limited, that is, proportional to $\exp(-E_{gap}/KT)$. The ultimate dark current performance is set by this diffusion limit, the most fundamental dark current mechanism. Diffusion current is a thermal mechanism where electrons and holes pairs are created in the bulk material and where the rate is proportional to the doping concentration. At a temperature of 100K the dark current is six orders of magnitude lower than that for an Indium Antimonide device such as the Aladdin detector. The plot also shows that the dark current doubles for every 1.7K increase in temperature.
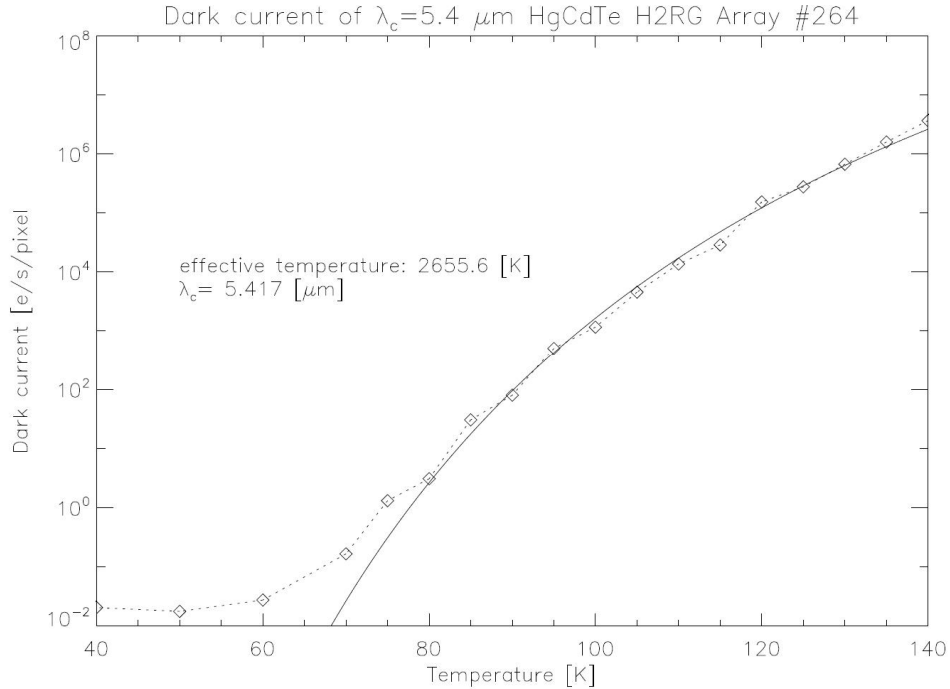

Figure 5: Dark current for our 5 um cut-off H2RG engineering device

4.2 Detector cosmetics

From the dark current plot we see that it is possible to operate this longer cut off detector at liquid nitrogen temperatures which is useful in simplifying instrument design. However the cosmetic quality of the detector does change with temperature as shown in Figure 6 where we have two bias images at different temperatures. It is clearly seen that is very advantageous to operate the detector below liquid nitrogen temperatures.
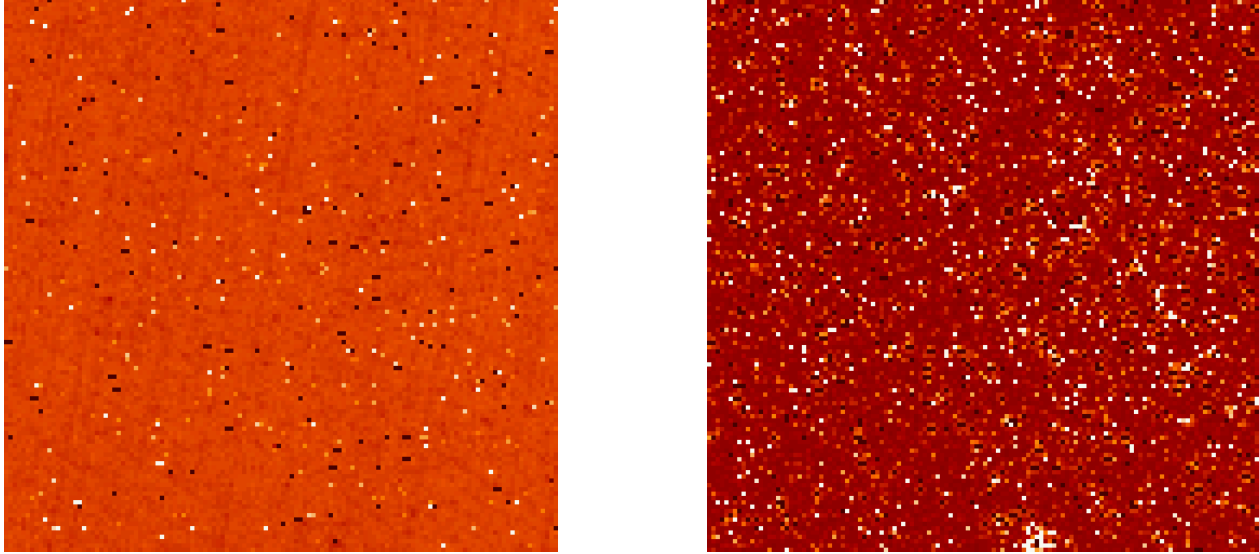

Figure 6: cosmetics as a function of temperature, left T=40K and right T=80K

4.3 System configuration for detector fast outputs

The HAWAII-2RG [7] multiplexer can be read out at a pixel rate of 5 MHz and faster. In this readout mode, an additional column wise sample-and-hold stage plus a programmable gain amplifier (column buffer) is used. This column buffer cell together with the horizontal read bus and the output buffer circuitry can be found in the detector technical manual but cannot be repeated here due to export regulations. The column buffer requires many additional bias voltages, the most important of which are Vnbias, Vpbias, Vncasc and Vpcasc. The fast output buffer is controlled by Vbiasoutbuf but for our configuration we use the unbuffered outputs. Detailed information about these voltages can be found in the Teledyne manual referenced above. The two reference voltages RefSample and RefColbuf are used in the sample-and-hold stages and allow the user to perform a level shift of the output signal over a wide voltage range.

It is very simple to switch between the slow or fast outputs, using the serial communication lines and simple programming of the on board registers. In our configuration we only use 8 clock lines for operation, namely, FSYNCB, VCLK, LSYNCB, HCLK, READEN, MAINRESETB, SAMPLECLK, CSB and RESETEN. We also reuse the FSYNCB line as the DATAIN line and the VCLK line as the DATACLK line, thus saving a further two clock lines.

We use 13 bias lines for operation, namely VnCase, VpCase, VnBias, VpBias, RefSample, Refcolbuf, Vbiasoutbuf, Vdd, Vdda, Vbiaspower, Vreset, Vbiasgate and Dsub. In our implementation we have had to reuse some clock lines as bias lines because of the lack of bias lines in the original pre-amplifier implementation. As already stated, programming of the registers to select slow or fast outputs is relatively simple, the main issue to be concerned about is how does one know what output has actually been selected, except for working through all the programming code. The simple solution is to look at a spot image projected onto the detector. The analogue output voltage is inverted in fast output mode compared to the slow mode. This is most easily seen in Figure 7 which is an image of such a projected spot, all else being the same except the choice of outputs. The image also shows that the gain is approximately the same in this configuration for both slow and fast outputs. In our setup the internal gain registers have been programmed to give an internal gain of one.
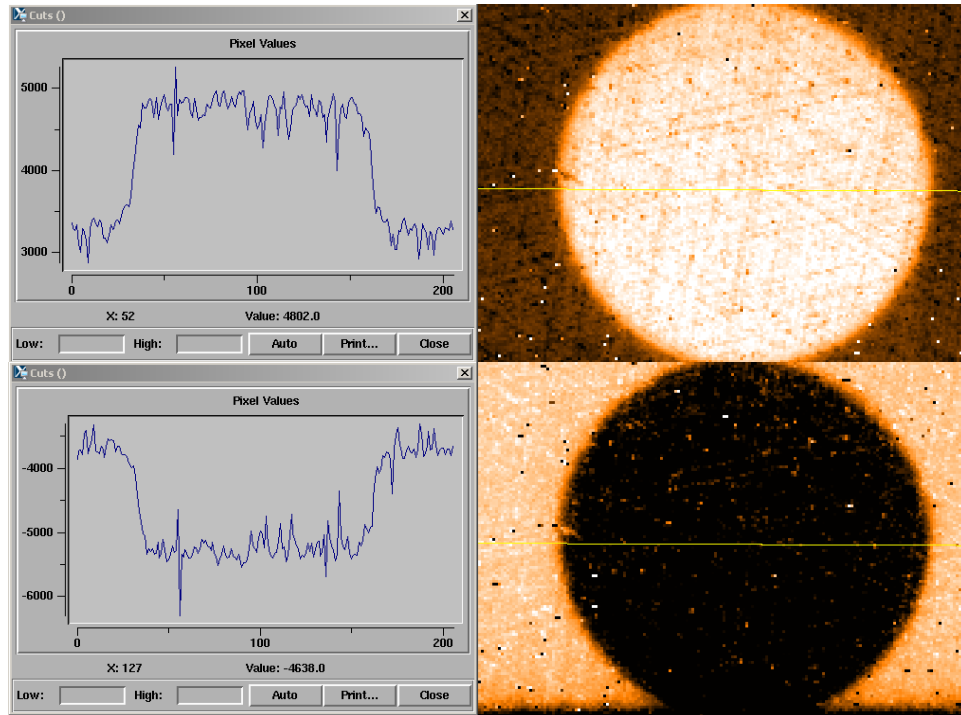
Figure 7: standard slow speed outputs (top), fast outputs (bottom) – shows inversion of signal when switching between output types

All of the bias voltages, associated with the column buffer cell, need to be adjusted to ensure optimal operation of the fast outputs. For our engineering grade device we find that the outputs are most sensitive to VnBias, DSub and Vreset, with the circuitry only working optimally within a few tens of millivolts of the optimal set point for the VnBias voltage. Figure 8 shows images of the detector when performing a sweep of this voltage and highlights the sensitivity of the fast outputs to this one bias voltage. Most of the other biases are set to the default values described in the manual. However we also have had to offset the Dsub and Vreset bias voltages from those values used for the typical setup for our slow outputs. There is some cause for concern in that any drift in the VnBias voltage may actually move the fast outputs out of range whilst in operation since only a few tens of millvolts has been shown to do this. More optimization is required to try and ensure a point of operation where less sensitivity is seen. When operating with the slow outputs then the extra bias voltages are kept in their default state with no effect seen on the slow output performance.

4.4 Read out performance

At present with our NGC system we are limited in how fast we can read out the detector. We have a 1 MHz, 32 channel ADC board and a plug in replacement 3 MHz board. However because of some issues with the faster board we cannot read a pixel much faster than approximately 2.0 Mpixels/second. The main issues are with capacitance in our long flexi cables and some noise issues with the board itself. Also for our testing we have been conservative in our pre-amplifier design and used only the OPA4530 devices which are not actually quite fast enough for the large signal swings from the detector. At 2 MHz operation with hot pixels we are seeing some inter-pixel modulation which is probably due to the slew rate limitations of these op-amps. A future test will use the OPA4354 op-amps which are a much better match to the fast outputs of the H2RG detector. However we can still do a comparison of the fast outputs against the slow outputs in terms of noise and also noise versus pixel speed for the fast outputs.
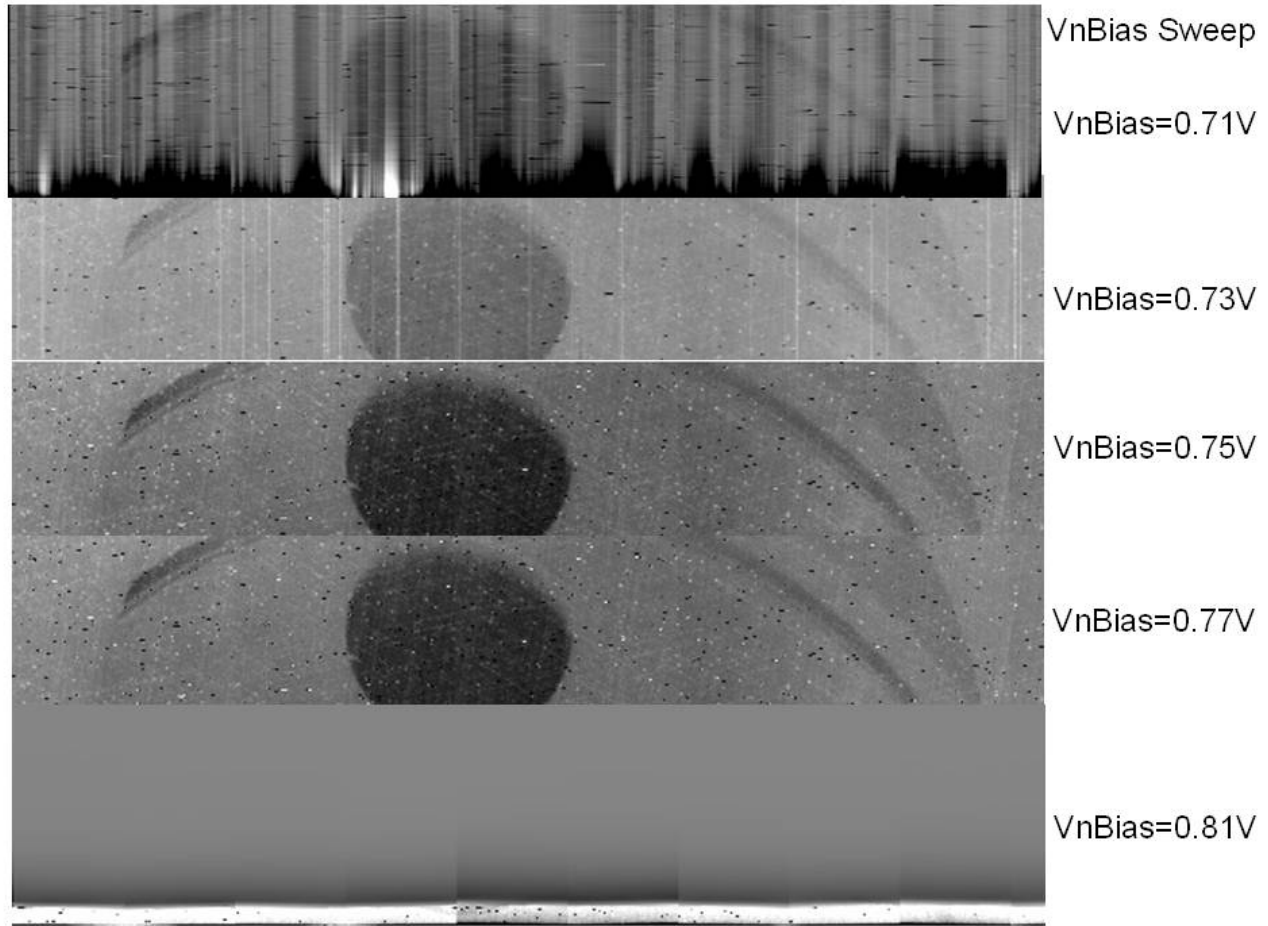
Figure 8: VnBias voltage sweep (top 0.73V, 0.76V, 0.77V and 0.81V bottom)

To carry out detailed testing the detector setup has four defined regions. There is a bias shift about one third of the way in the x direction as shown in Figure 9. This is because the first twelve outputs use the slower TLC2274 op-amps whereas the remaining twenty outputs use the faster OPA4350 op-amps. This configuration allows us to compare the performance of the faster circuitry against the ESO standard configuration. Likewise there is a bias shift at approximately the half way mark in the y direction. This is because the top half of the detector is masked off with a cold cover whereas the bottom half is able to see out of the cryostat into our blackbody source. This then allows us to easily do read noise and photon transfer measurements. This masking of the detector was required because our test camera setup does not have a cold stop, this together with the fact that the detector is sensitive to 5 um radiation means that dark current and noise measurements would be impossible otherwise. We also had some issues with filters warming up/cooling down when moving to position which meant that we needed some settling time after changing a filter. This filter stability issue will have some effect on the linearity measurements.

The slow outputs are typically operated at 100 kHz or approximately at one full frame per second. However by increasing the current to the pixel source follower by lowering Vbiasgate to 2.3V, they can be operated twice as fast through these slow outputs. The detector can be operated at 500 kHz pixel and beyond but with serious inter pixel modulation issues. The read noise for the slow outputs in our engineering detector is approximately 9 e rms for a simple correlated double sample exposure. The read noise for the fast outputs is approximately four to five times higher than the slow outputs and is approximately 40 e rms measured at the slow pixel rate with the same system bandwidth.

Fast Outputs Read Noise ~ 4 x Slow Outputs Read Noise at 100 kHz pixel operation

The read noise of the fast outputs also reduces by approximately a factor of three with increasing numbers of Fowler pairs as shown in Figure 10. Figure 10 also shows a linearity plot for the detector using the high speed outputs. The linearity has been measured to better than 5% up to 90ke signal level. The non-linearity has been calculated by subtracting the real measured values from the linearity slope. No account has been taken here of transimpedance conversion gain changes versus signal level due to capacitance changes in the unit cell diodes but the linearity is good in any case. Correcting for the gain versus signal will help to further improve the linearity. The transimpedance conversion gain is similar to within 20% for both slow and fast outputs and is approximately 4 uV/e for this detector using the fast outputs and internal gain set to one. The dynamic range of the fast outputs also seems to be similar to the slow outputs in that a full well signal of greater than 100 ke can be measured on the fast outputs.
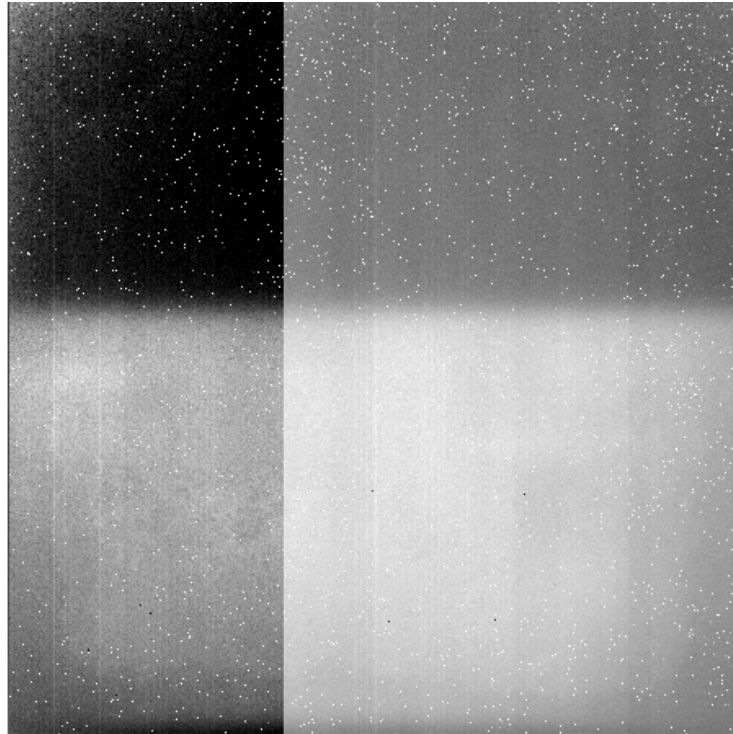

Figure 9: Single Reset-Read Bias image showing 4 distinct regions (top region is cold shielded, bottom open, left side uses slow op-amps, right side uses fast op-amps)

The conversion gain for each of the plots given in Figure 10 is approximately 4 e/DN. All linearity and gain measurements were taken using a simple black body viewed through a set of cold filters. As already mentioned, when a filter is moved then its temperature is seems to change. This is seen by the fact that the signal slowly creeps upwards after a new filter has been selected.
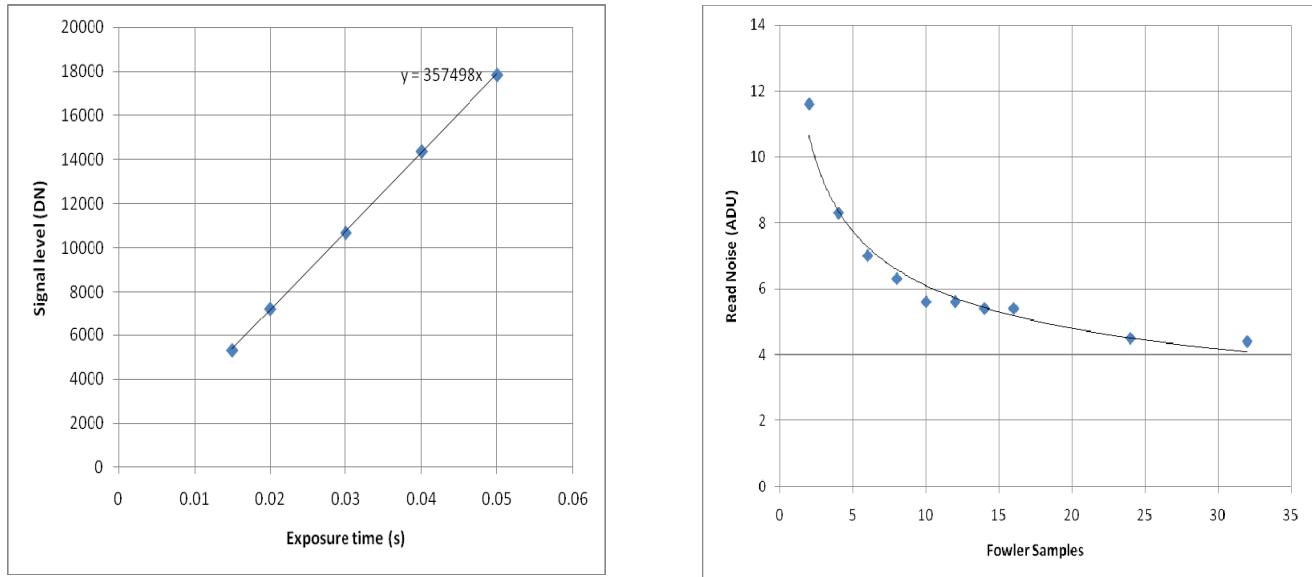
Figure 10: Linearity plot for fast outputs (left) and noise versus Fowler pairs (right)

5. CONCLUSIONS

The HAWAII-2RG detector has now been operated using the fast outputs and the data analyzed to determine if it is useful for astronomical applications. To program the detector to operate in this mode has been shown to be reasonably simple. In our NGC setup, it is a simple matter of pressing a button on a GUI to select between slow or fast outputs. Many extra biases are required for the new faster operation but the number of clocks can be minimized by re-using the same clock lines both for clocking and the serial data link for register programming. However, even with the use of faster op-amps, our hardware is not optimized for running at highest pixel speeds. We adopted an approach of changing op-amps on our cryogenic preamplifier board which was originally designed for 100 kHz operation, rather than doing a new high speed PCB design. To reach the full speed potential of an H2RG detector at high speed will require either the use of the ASIC with the detector positioned very close to it or the design of a new cryogenic preamplifier which is much more optimized for high speeds. This will mainly entail the minimization of capacitance on the video lines between detector and op-amp inputs as well as impedance matched cables at the outputs. T

The read noise of the fast outputs has also been determined. It is typically a factor of four times higher than for the slow outputs when operating in the 100 kHz standard regime. This makes the detector when used with these outputs much less useful for astronomical spectrometry applications where read noise is usually always the dominate noise source. The detector can also be operated through the slow outputs at pixels rates twice that advised in the technical manual with little or no impact on read noise. In other regards such as signal swing and linearity the fast outputs of the detector function in a similar manner to the slow outputs.

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