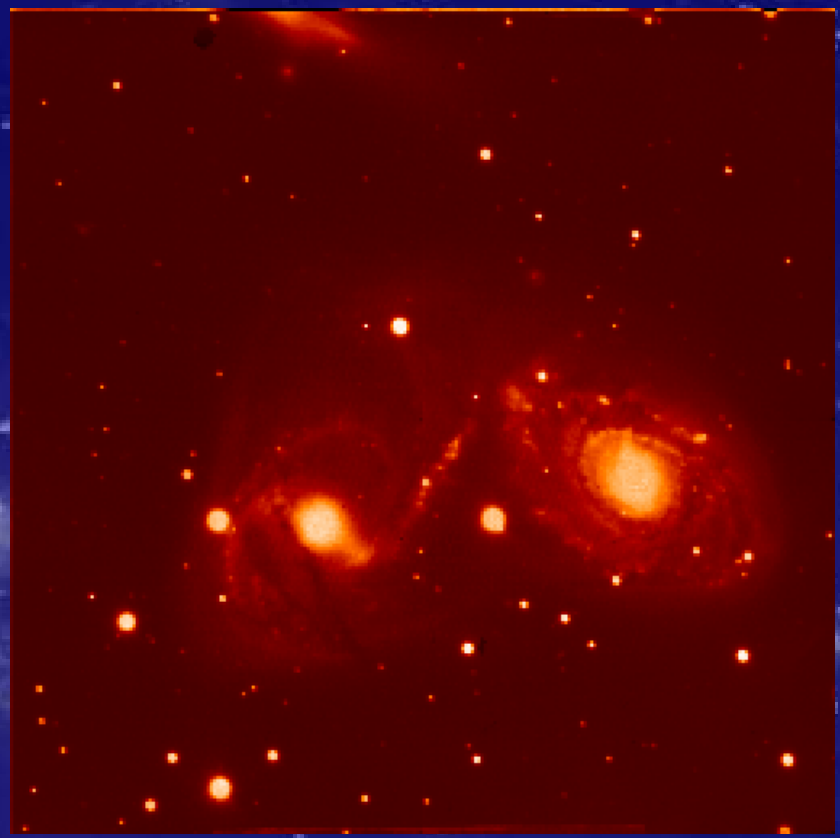
Prototyping NGC



First Light

PICNIC Array Image of ESO Messenger Front Page

Introduction and Key Points

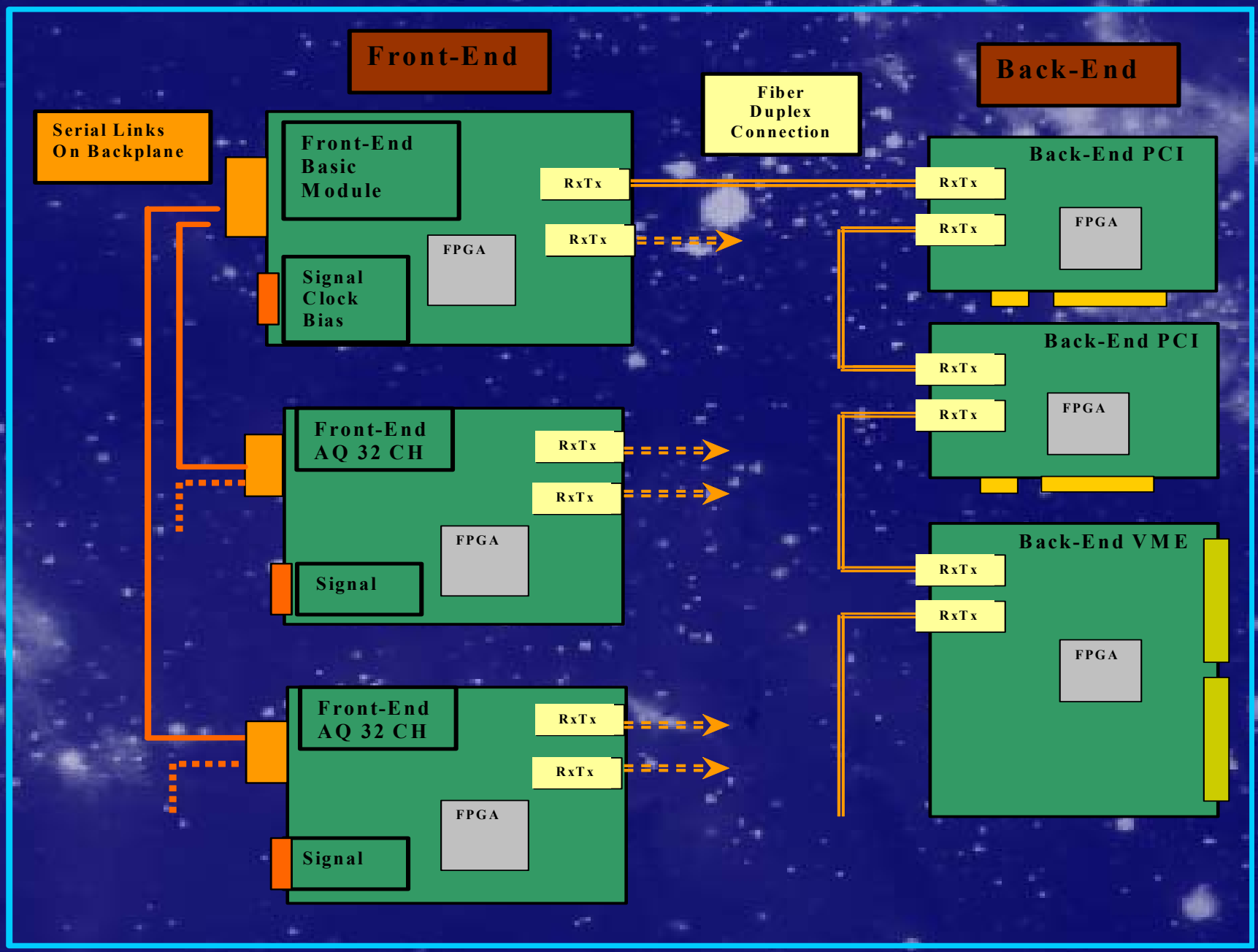
Constructed is a modular system with :

A Back-End as 64 Bit PCI Master/Slave Interface

A basic Front-end unit containing a four channel system on one card of standard VME 6U size.

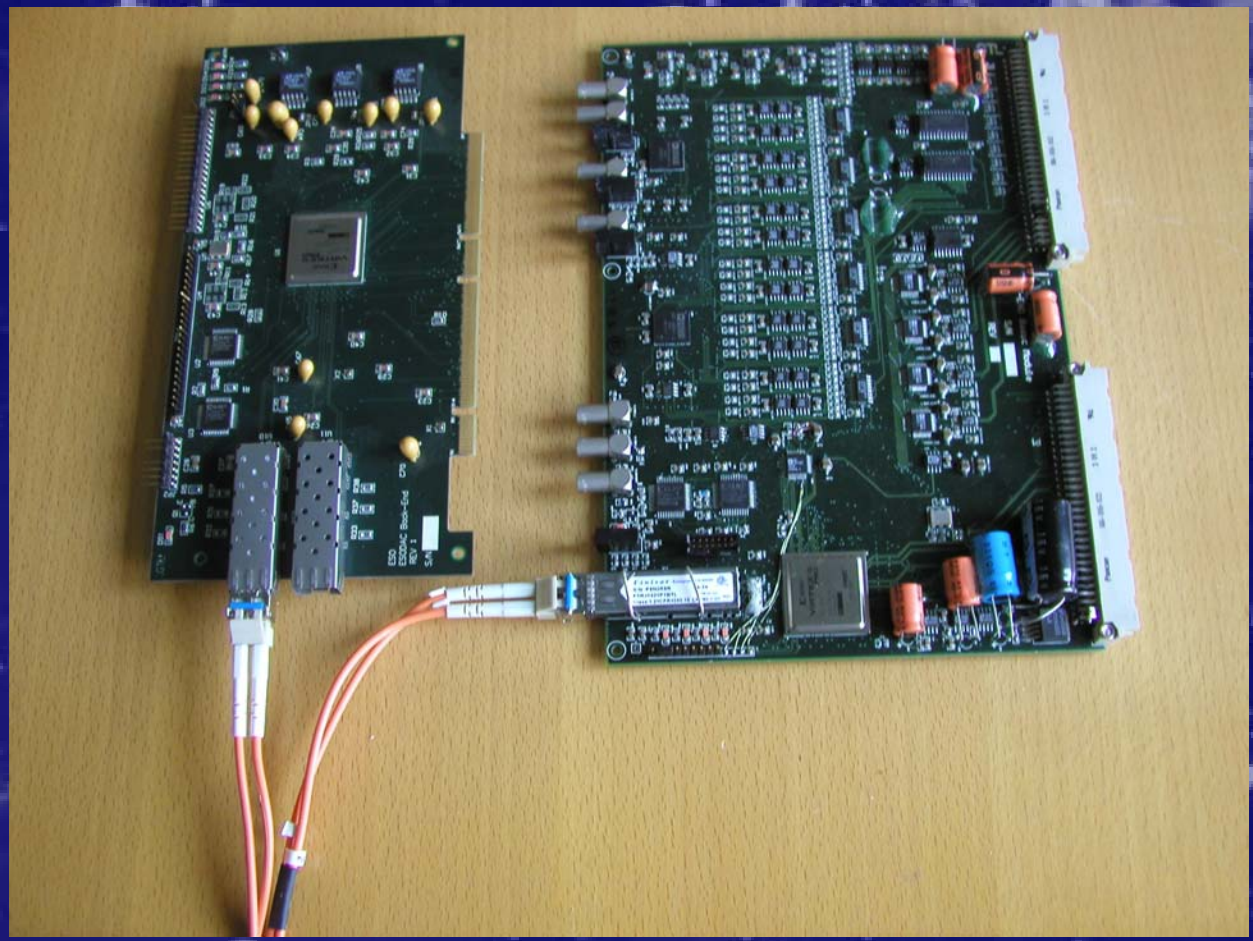
- Power Consumption on this Front-end is less than 10 Watts (Excluding power supply)
- Very low noise achieved, because there is no processor, no data bus on the front-end side.
- Data distribution on Back and Front-end side possible – free topology .
- Connection between Back and Front-end only by fibers.
- System does not require active cooling.

System Block



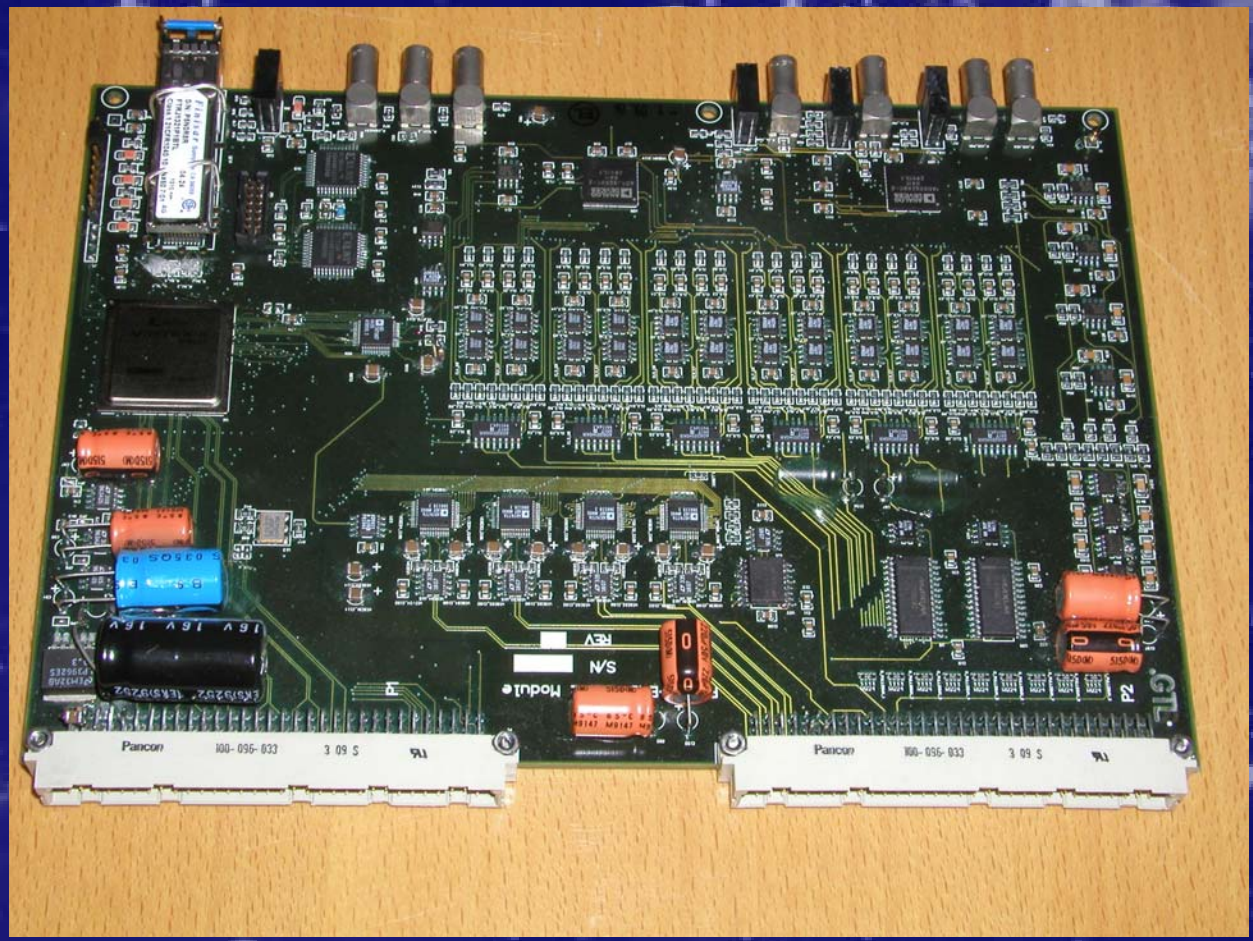
Real Hard Ware

Minimum System
Back-End and Front-End (Four Channels)

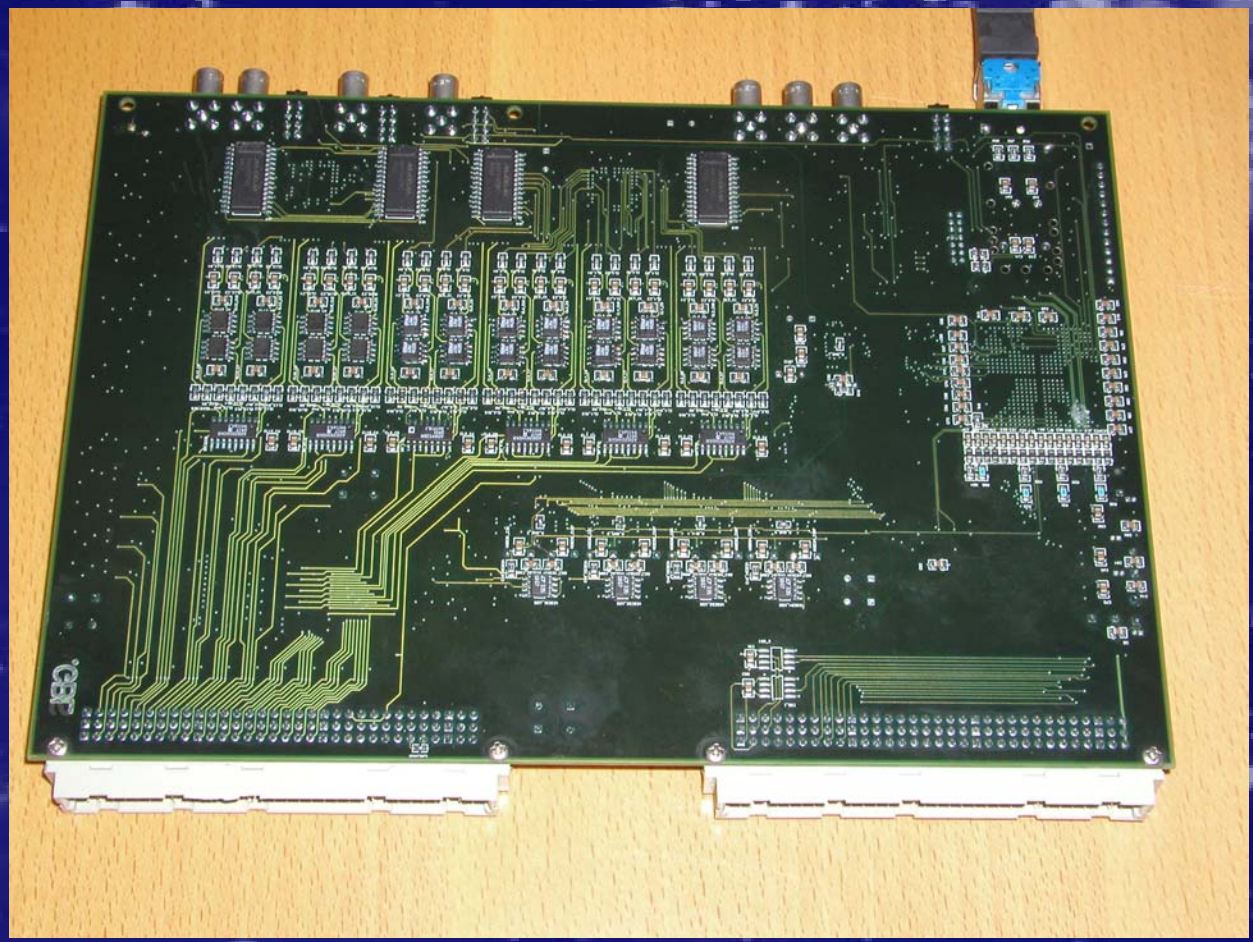


Back-End

Front-End (Four Channels)



Front-End (Four Channels)



Virtex Pro Facts

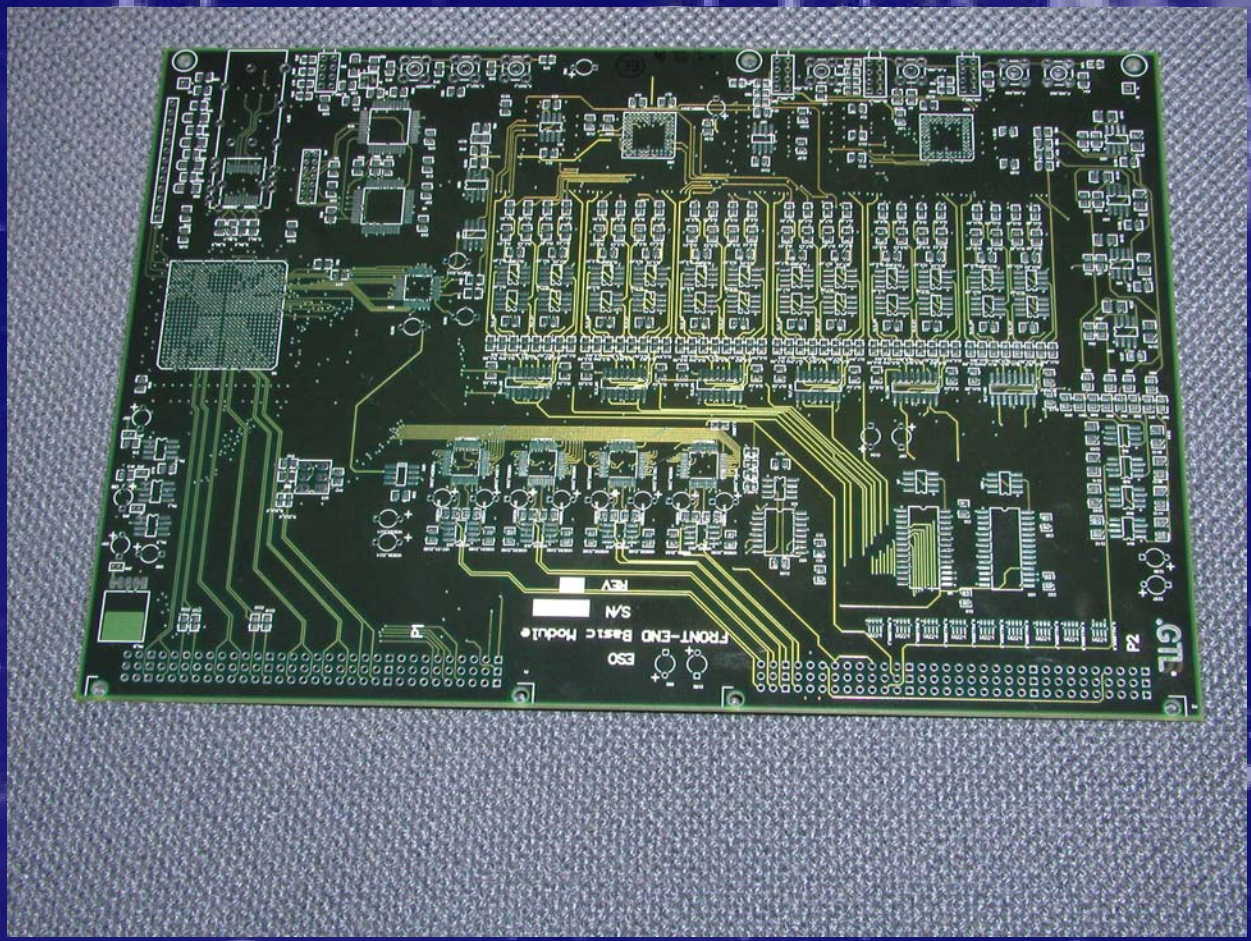
Device utilization summary: Selected Device : 2vp7ff672-5

Number of Slices:	2508	out of	4928	50%
Number of Slice Flip Flops:	3043	out of	9856	30%
Number of 4 input LUTs:	4190	out of	9856	42%
Number of bonded IOBs:	124	out of	396	31%
Number of TBUFs:	160	out of	2720	5%
Number of BRAMs:	25	out of	44	56%
Number of GCLKs:	3	out of	16	18%
Number of GTs:	4	out of	8	50%
Number of DCMs:	1	out of	4	25%

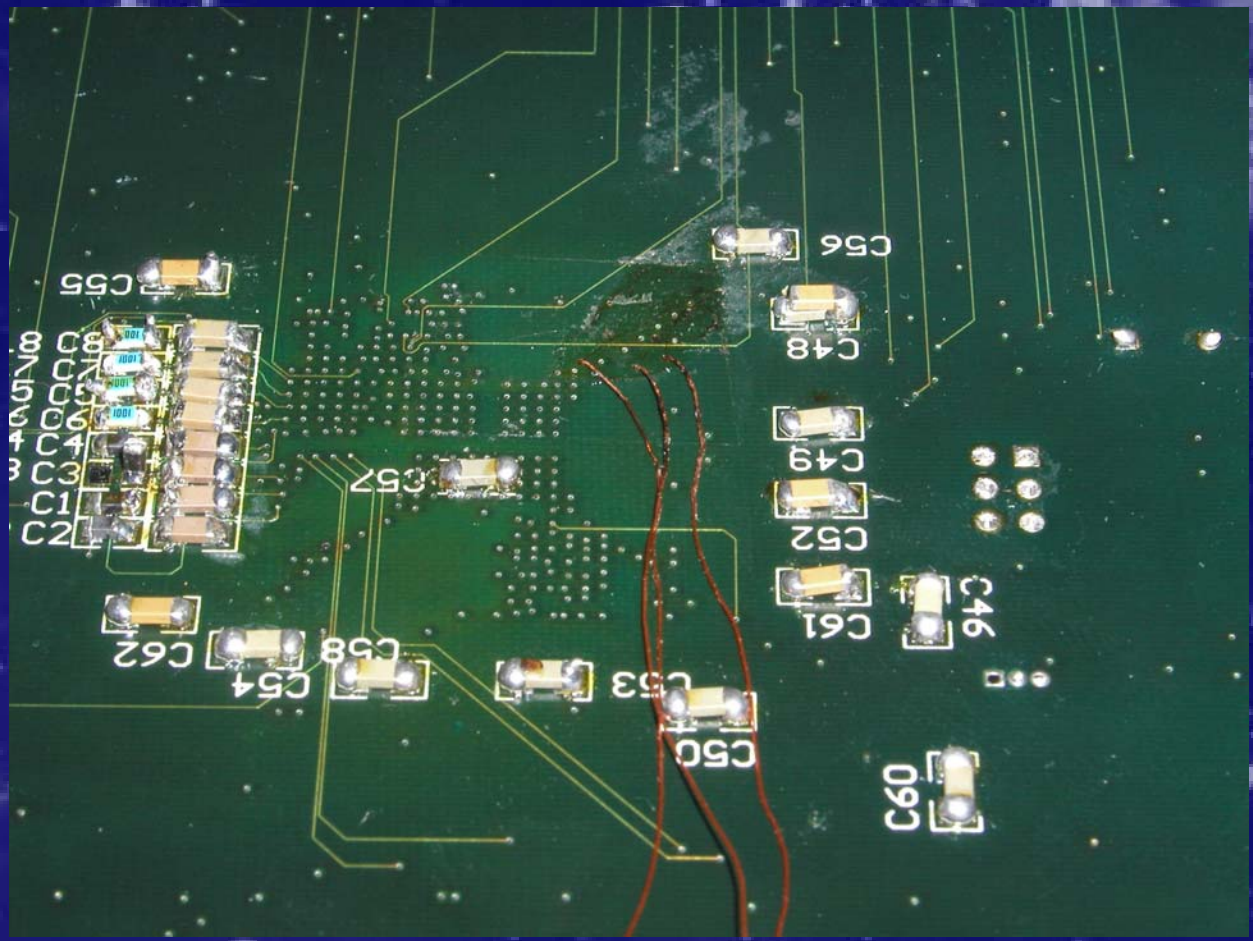
Signals to route : **22530 !**

Engineers Bad Days

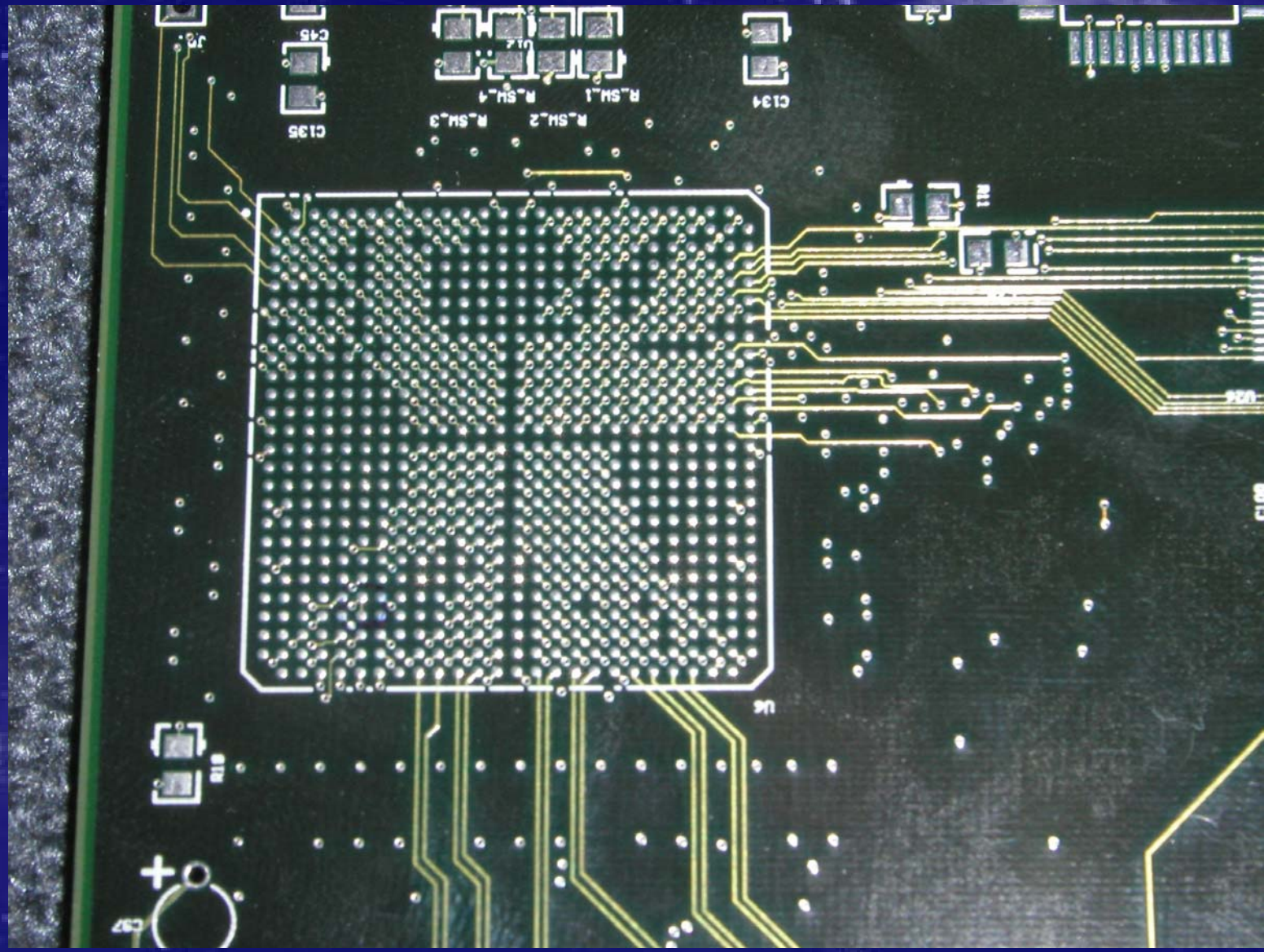
How many Errors will be on ?
It's a 10 Layer board !



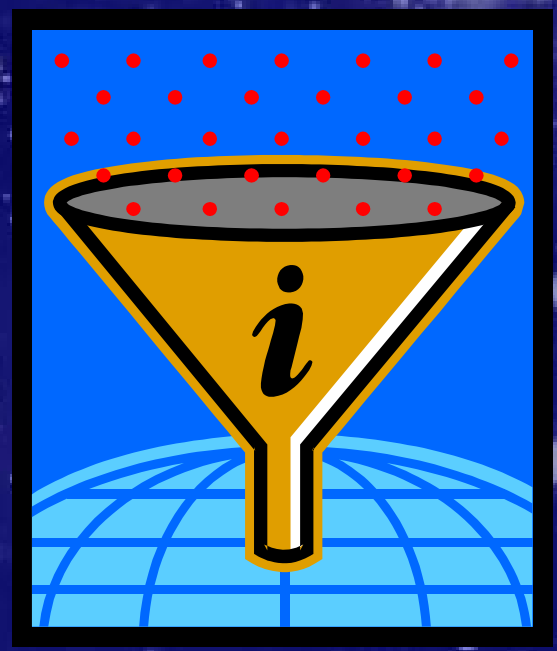
Virtex BGA - Missing Connection



Virtex BGA - One Connection too much



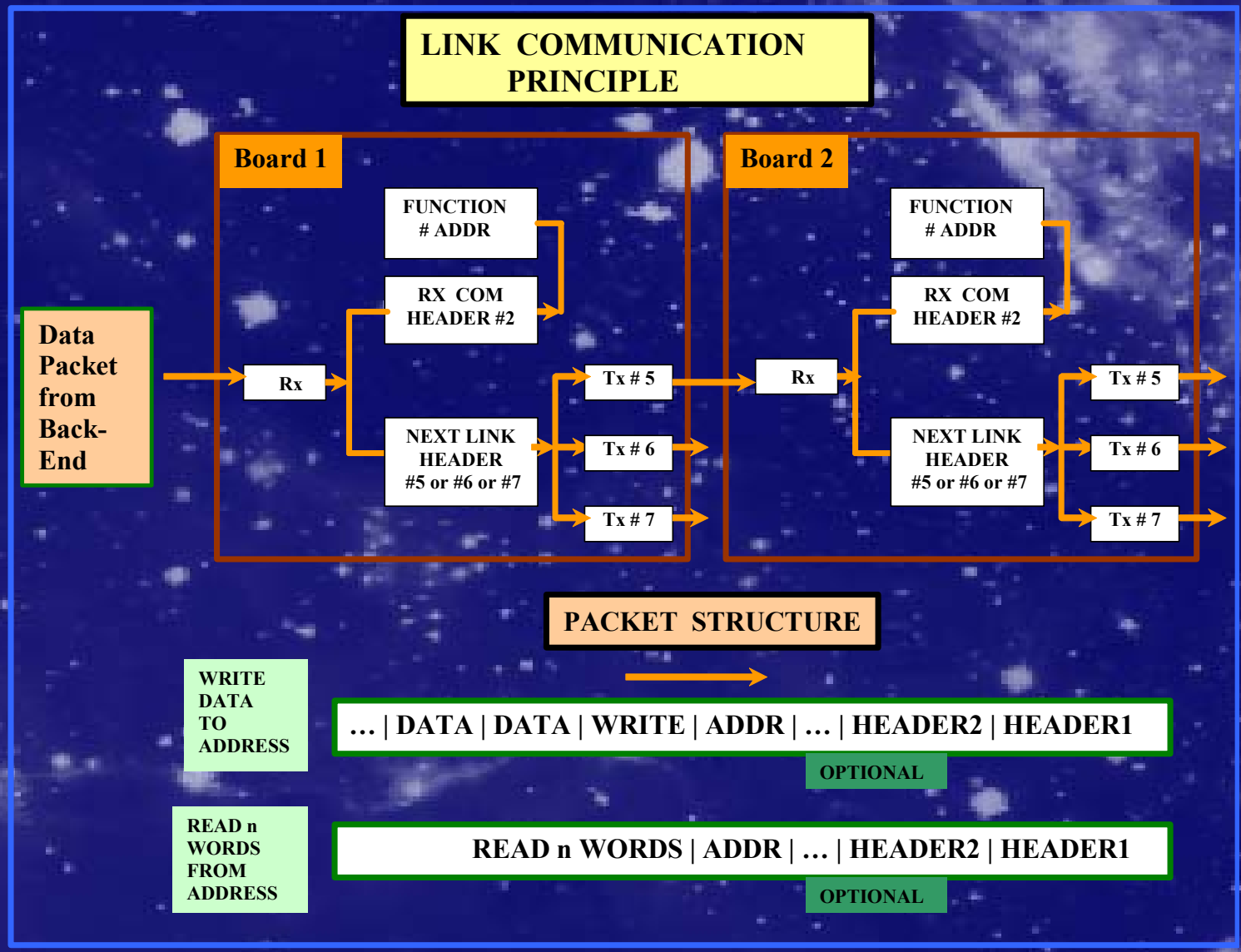
System Design and Status



Structure
Communication and Data Transfer

- Communication and data transfer to the back-end is handled with the Virtex Pro FPGA's Gigabit transceivers
- The physical transfer is handled either on fiber (Front-End to Back-End) or copper (within Front-End)
- The communication between all system modules is based on packet transmission over serial links
- The principle of communication is the same for all modules
- A packet structure is defined to address a function (e.g. a register or memory in a front-end module) for read or write
- From the Back-End (PCI board) the packets can be routed to and through each board in the Front-End
- Data are routed with the same structure from the acquisition modules to the Back-End
- In the Back-End a PCI DMA controller is implemented for transfer to the Acquisition computers memory

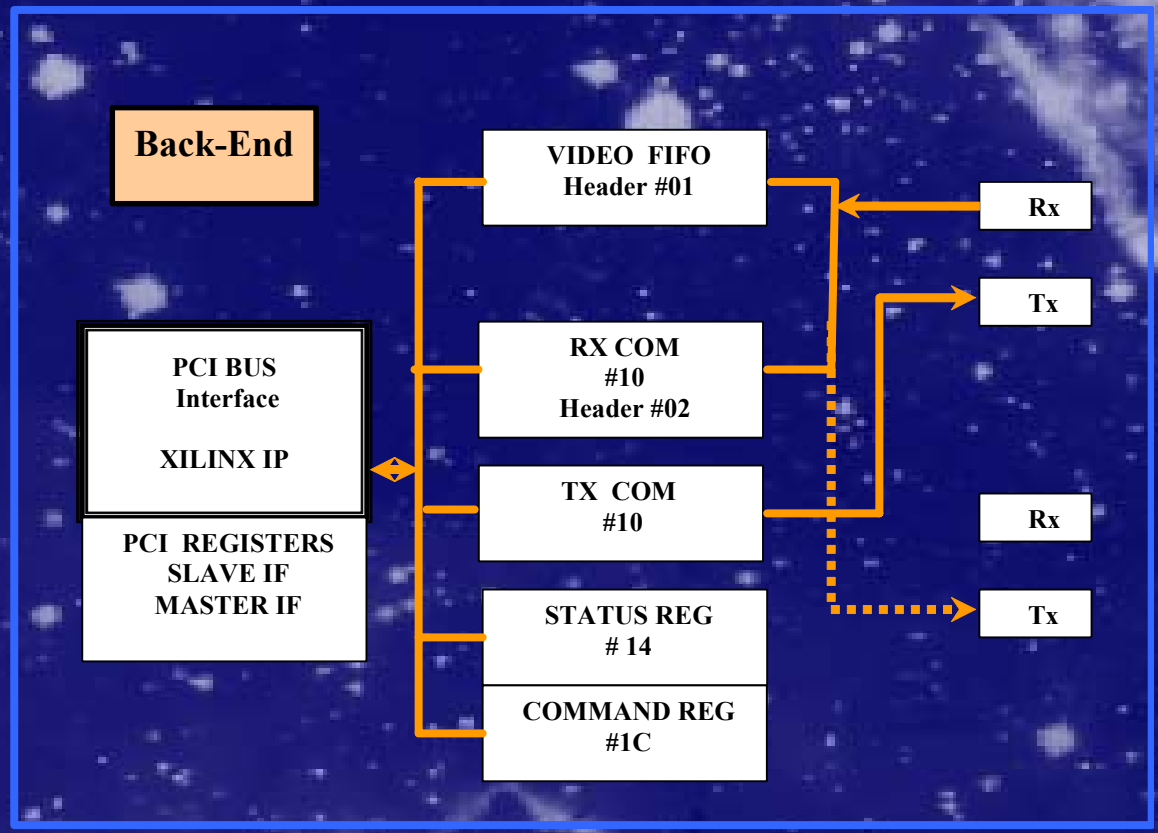
Communication and Data Transfer



Back-End

- Function is based on the XILINX Virtex Pro FPGA XC2VP7 FF 672 .
- Back-End PCI is a 64 Bit PCI board.
- FPGA contains PCI interface, protocol function PCI to transmit/receive buffer for communication and data reception and RocketIO transceivers.
- Direct interface from FPGA to PCI without glue logic.
- Independent PCI master and PCI slave.
- Communication and data transfers all on serial link
- Handshake communication to Front-End
- Data rate on one channel between front and back-end ~ 200MByte

Back-End

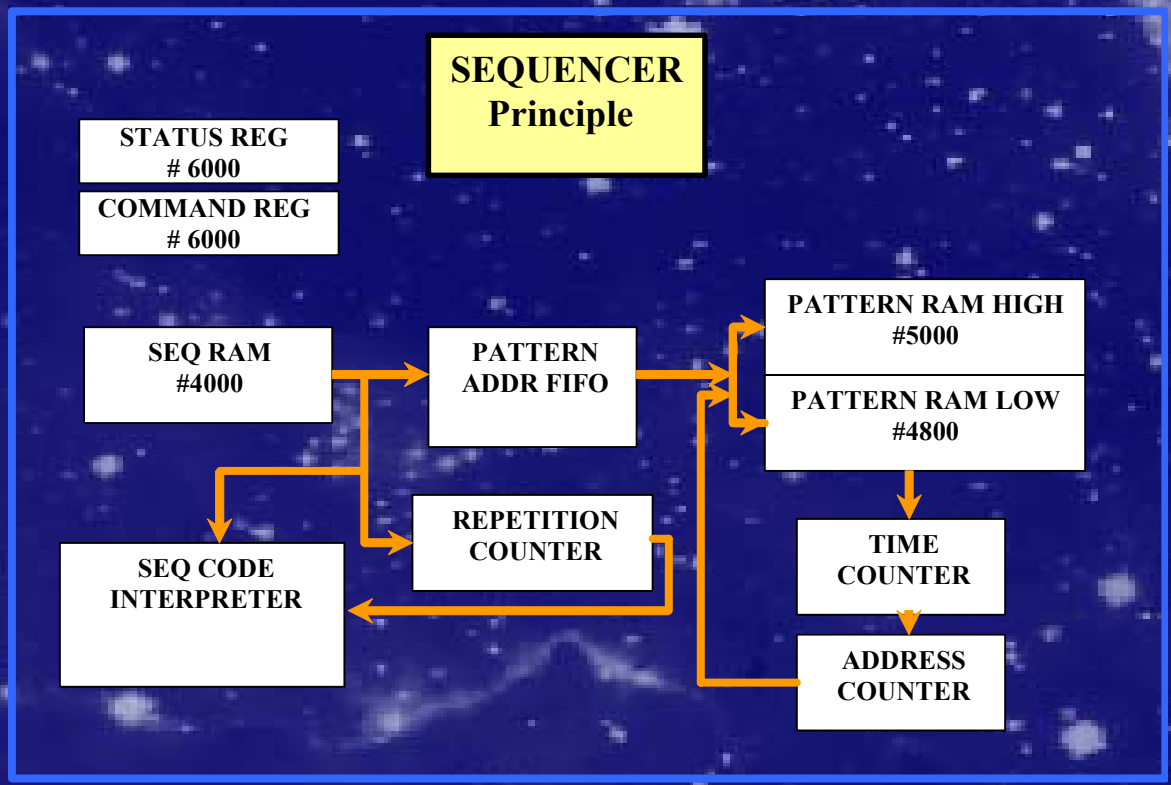

Back-End
VIDEO FIFO
Header #01
Rx
Tx
PCI BUS
Interface
XILINX IP
RX COM
#10
Header #02
TX COM
#10
Rx
PCI REGISTERS
SLAVE IF
MASTER IF
STATUS REG
14
Tx
COMMAND REG
#1C

Front-End Basic Board
Sequencer Module

- Sequencer is completely contained within the FPGA
- 100MHz design = 10ns resolution
- Interpreter for Sequencer Codes within the FPGA
- Galvanic isolated high speed trigger input and control outputs
- Sequencer Codes

000	Reserved	No Operation – Ignored
001	EXEC Pattern	< Number of Pattern, Number of Repetitions >
010	LOOP	< Number of Repetitions >
011	LOOP END	
100	LOOP INFINITE	
101	JUMP SUBROUTINE	< Address >
110	RETURN SUBROUTINE	
111	Reserved	No Operation – Ignored

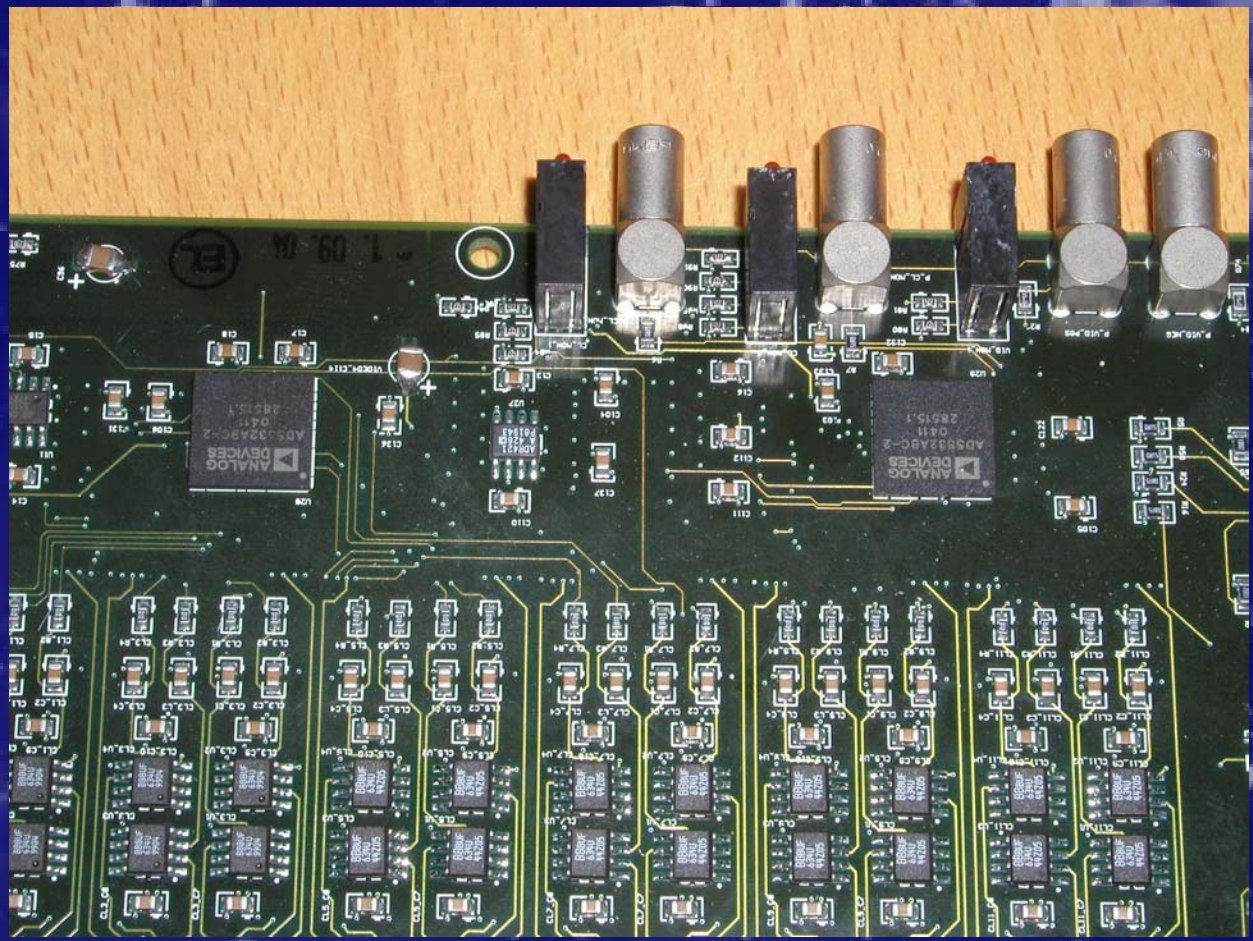
Front-End Basic Board
Sequencer Module



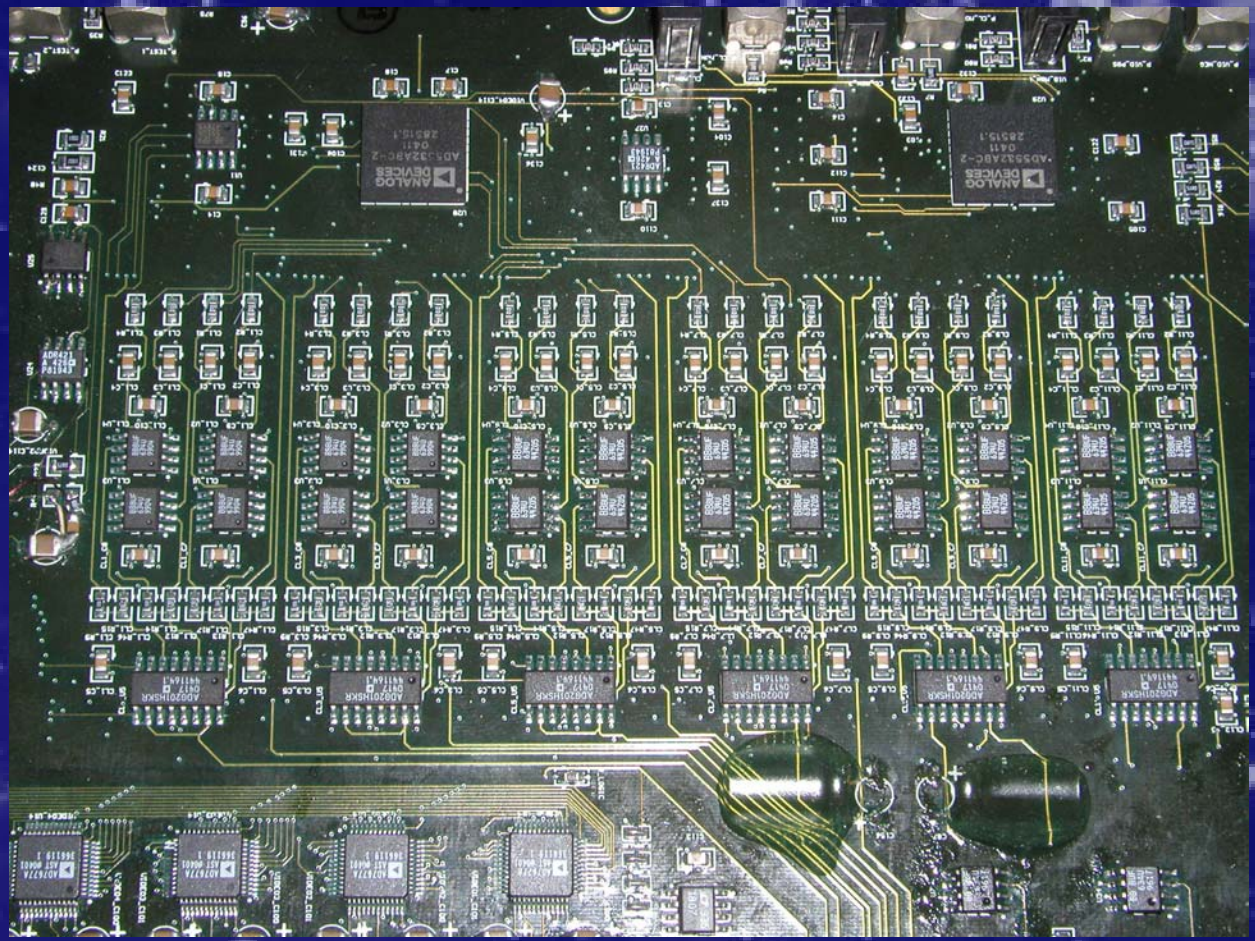
Front-End Basic Board
Bias and Clock Module

- 32 Clock Biases fully programmable
  within +/- 13 Volt span – resolution 50mV
- 12 Clocks
  Rise/Falltime (no load) 30ns
  Drive Peak 50mA, Cont 25mA
  Impedance 50 Ohm
- 4 Clocks
  Rise/Falltime (no load) 60ns
  Drive Peak 200mA, Cont 100mA
  Impedance 50 Ohm
- 16 DC Biases fully programmable
  within +/- 13 Volt span – resolution 50mV
  Drive Peak 50mA, Cont 25mA
- 4 DC Biases fully programmable
  within +/- 25 Volt span – resolution 100mV
  Drive Peak 200mA, Cont 100mA
- Telemetry for voltage and current with 16bit accuracy
  for clocks and biases

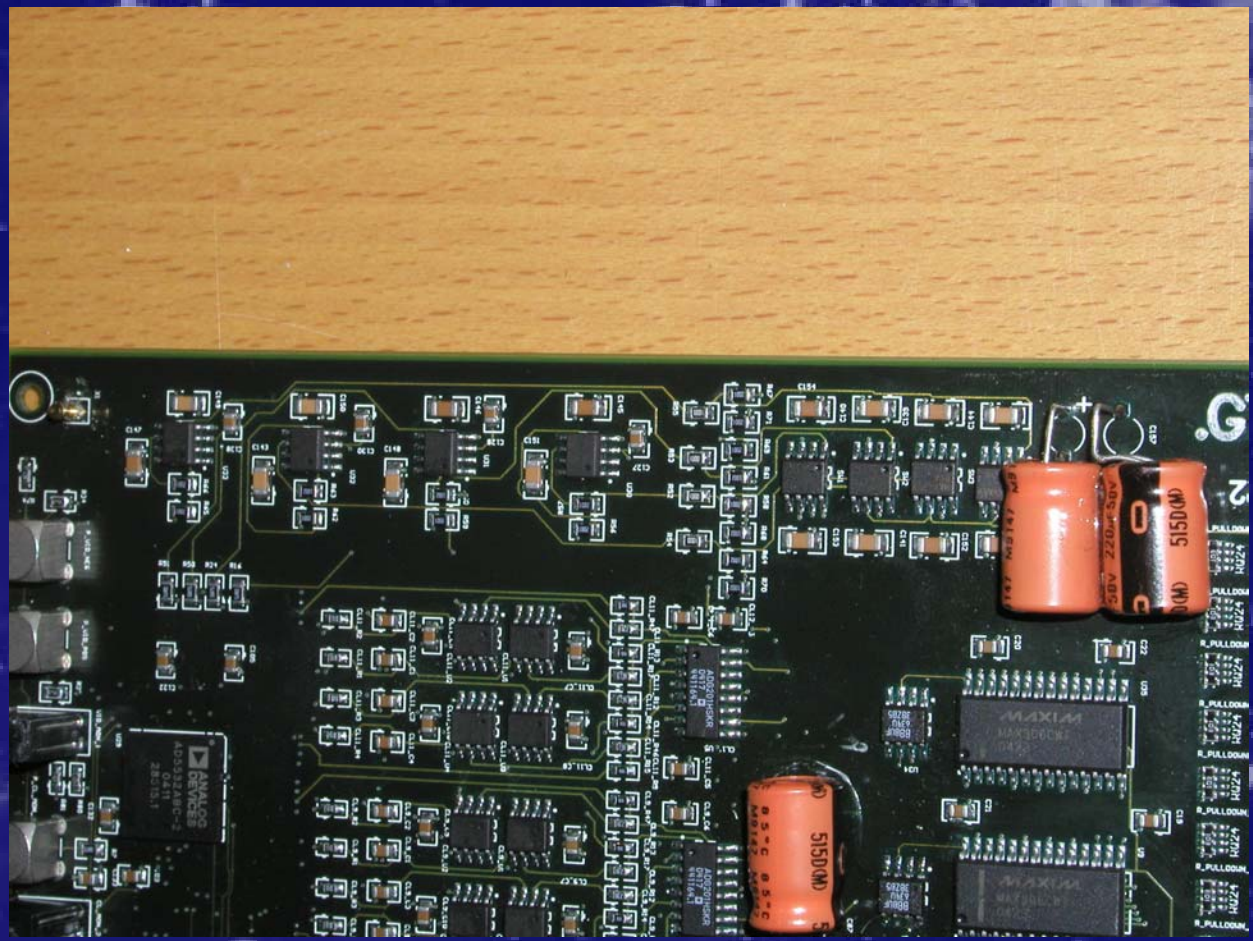
Bias DAC's



Clock and Bias



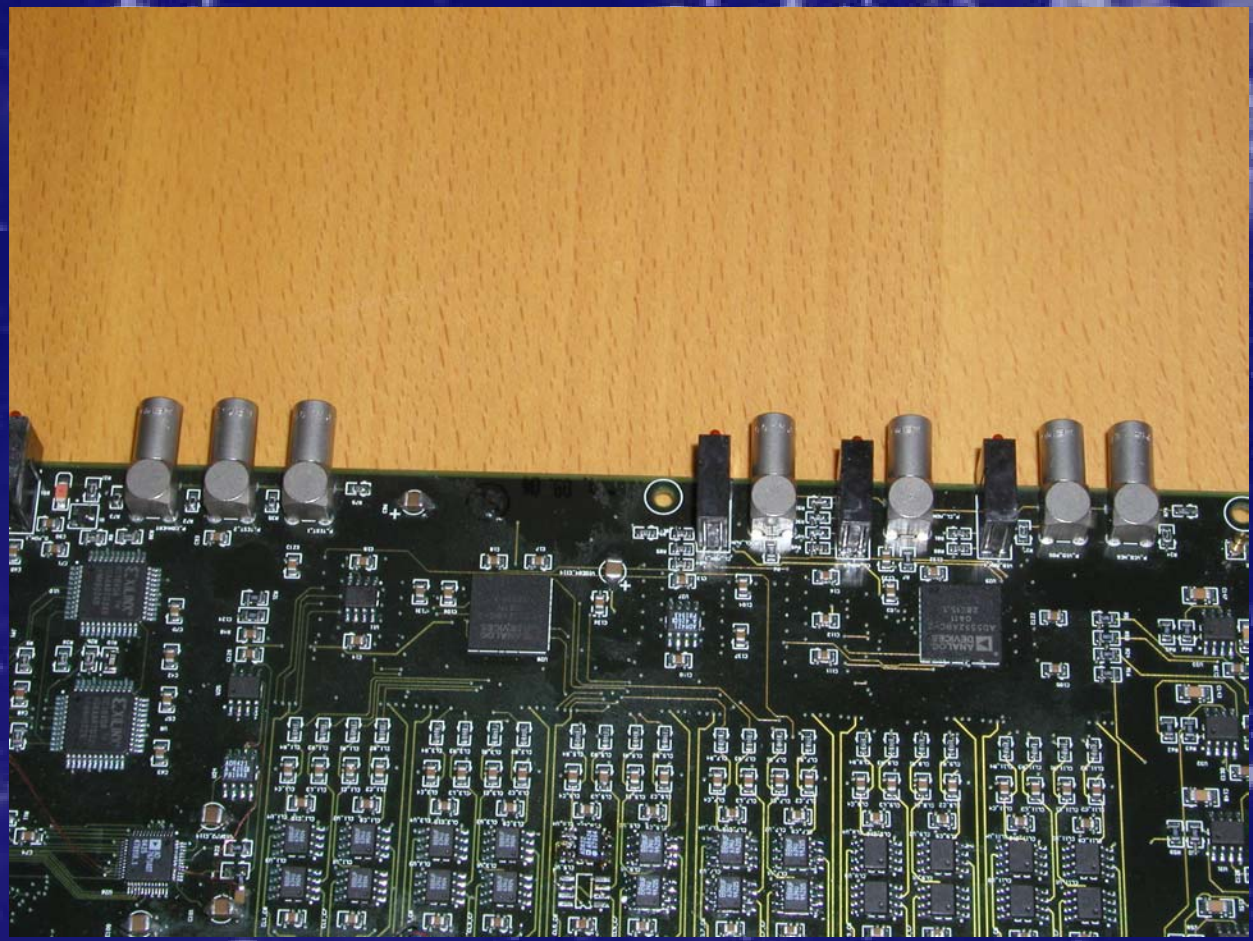
High Voltage/Current Bias



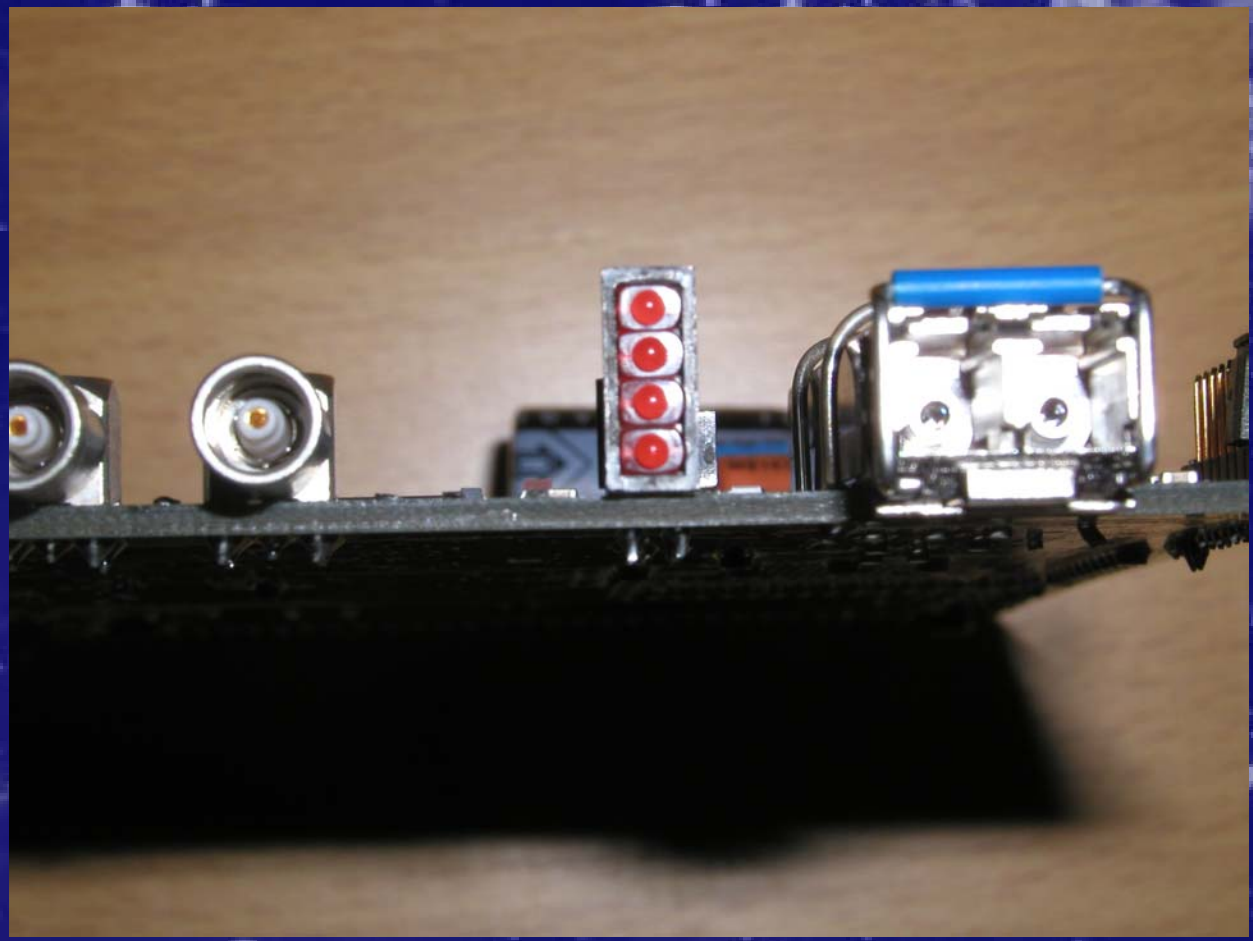
Front-End Basic Board Monitor Module

- All Monitor signals are available as LEMO outputs on front-panel Channel selection by software
- Monitor for differential video signals
- Monitor for conversion strobe
- Two clock monitors
- Two monitors for digital marker signals (Sequencer derived)
- LED's for Rx Tx Bias Enabled Sequencer Running

Monitors



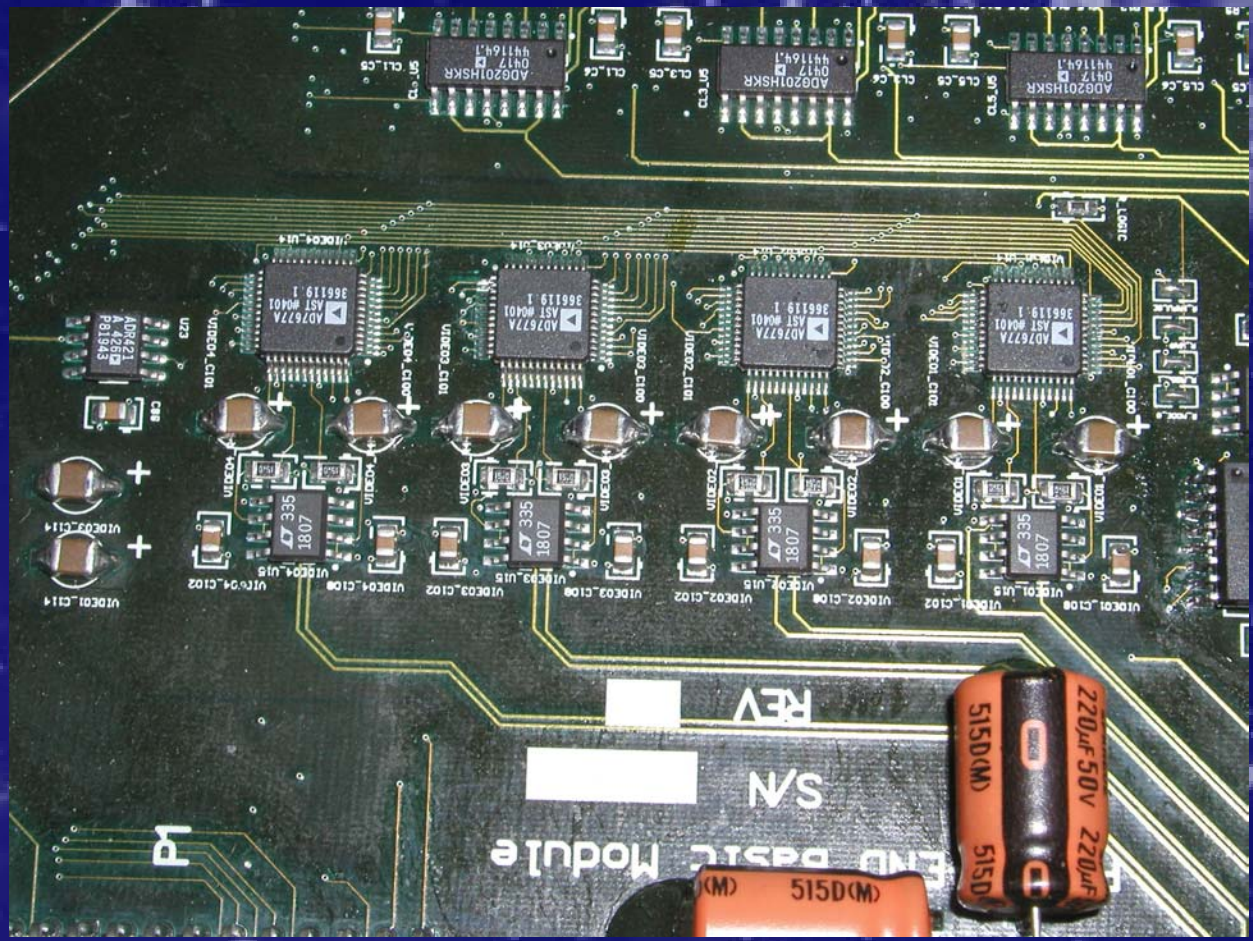
Monitor LED's



Front-End Basic Board
Acquisition Module (Four Channel)

- Routing of video data through a chain of boards
- Set-up of number of video channels
- Simulator of video data
- Software adjustable conversion strobe delay to accommodate preamplifier delay in 10ns steps
- Different ADC types have been incorporated
  - Standard – AD7677 (16bit 800KS) - RMS 0.5 ADU
  - High resolution – AD7674 (18bit 800KS) - RMS 0.5 ADU
- Possibility to incorporate high speed ADC's
  - High resolution – AD7674 (18bit 2MS)
  - Standard – AD7641 (16bit 3MS)

Acquisition Channels



Front-End Basic Module
External System Connections

- Synchronization to additional Basic Modules for
  - more clocks, biases
  - synchronized operation of different detectors
- External trigger input and control outputs
- For high-drive clocks (e.g. high capacitive loads by mosaics) provisions to external drive modules
- Connection to additional multi channel AQ modules by fiber or copper on high speed links with FPGA transceivers. This gives a very low "data bus" noise coupling to the analog part of the boards.
- Additional fiber output on each module for routing of special frames or to increase bandwidth
- ? Connection to detector ASIC's with special board - all communication and data transfer to the back-end is handled with the same firmware already contained in the present controller ?

Under Construction

Under Construction

AQ 32 Module

- The front-end AQ 32 Module is also based on the XILINX Virtex Pro FPGA XC2VP7 FF 672.
- The same firmware (AQ manager and Communication VHDL program as already installed in the Basic Module) will be used
- On board are (at least ?) 32 acquisition channels on 16 Bits or 18 Bits
- ADC's are the AD7677 (16 Bits) or the AD7674 (18 Bits) from Analog Devices (partly Pin-out compatible)
- The preamplifier is fully differential, input range will be +/- 2.5V. There will be no clamp/sample implemented on the board.

AQ 32 F Module (F means fast)

- On the basis of the AQ 32 module a version with fast ADC's (3 MS on 16 Bit, 2 MS on 18 Bit) can be build. Same layout and printed board might be possible.

High Drive Module for high capacitive loads on clocks on big CCD mosaics

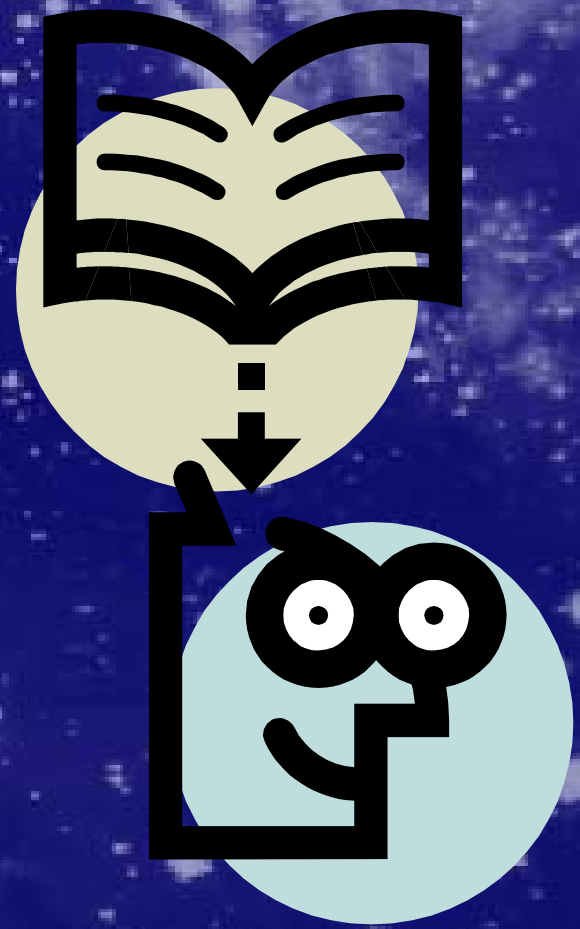
Power Supply

Preamplifier

Additional Tasks

- Implementation of TIM module into Back-End ?
  - Implement hardware on Back-End
  - Make VHDL design
- Revision of Front-End Basic Board
  - Revise Layout
- Power supply – Buy or Design and where located ?
- Mechanics, Enclosure

Outlook



Outlook

Use of NGC for Technical CCD's ? – Late but maybe useful

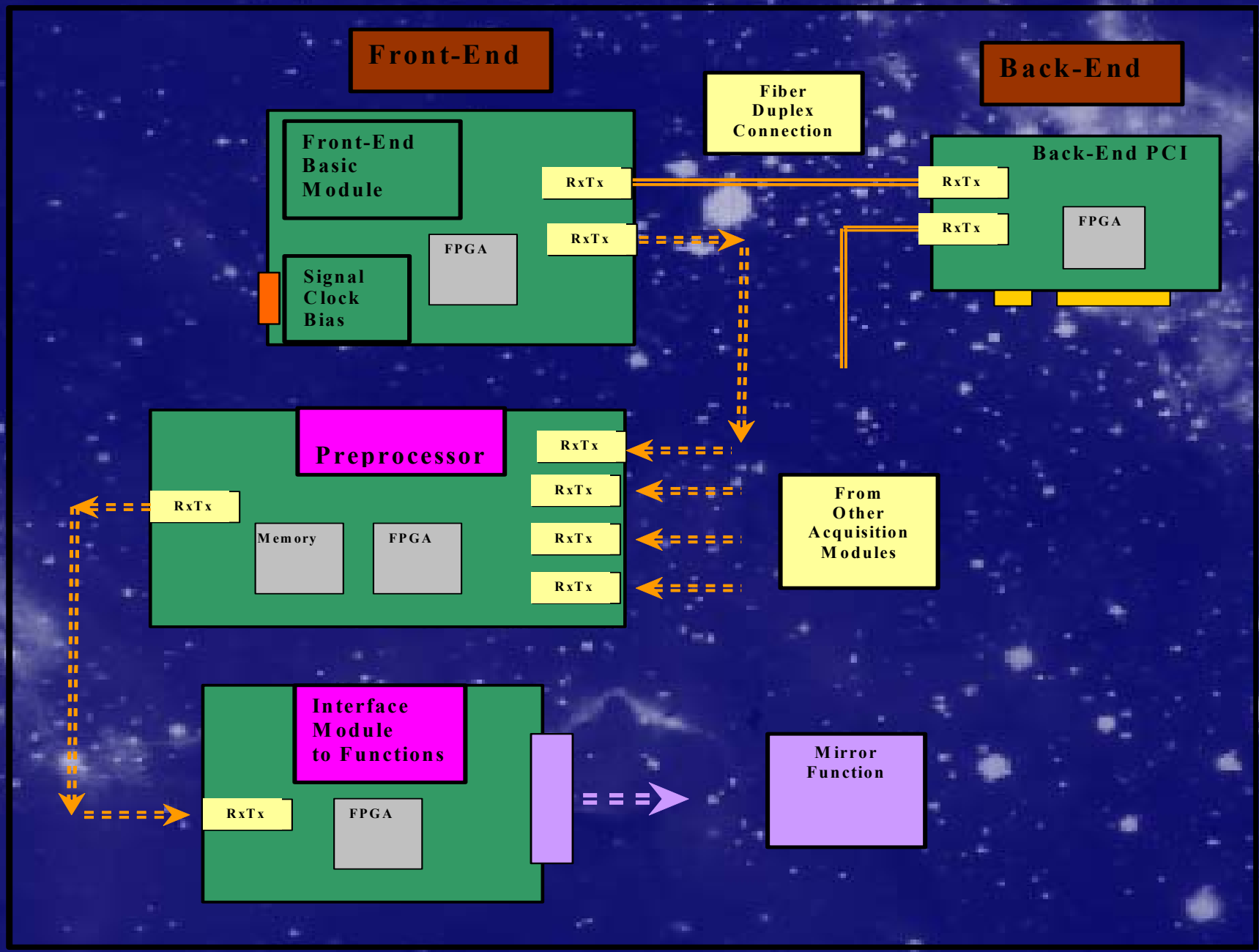
Because of the very compact design and the low power dissipation the Front-End Basic Module could be used for TCCD's. Advantages are a common platform for all types of detector data acquisition systems in hardware and software and no water cooling requirements for this system in sensible areas.

Outlook

Design of Real Time Processor for Adaptive Optics and Interferometry ?

- Data links from Acquisition modules could feed a very fast preprocessor (the Virtex Pro contains already Power PC(s) on chip) with data required for interferometry or adaptive optics.
- The whole control loop can be implemented within this Preprocessor, also the interface to the functions can be on this board.
- Because the only input to the board is the data fiber, the board(s) can be installed close to the function.
- Routing of acquisition data can be easily accomplished.
- The Virtex Pro chip can contain up to four Power PC processors ! Future XILINX chips (V4) with even higher density and higher speed are already in production. Links are compatible with links of NGC prototype.
- VME would no more be needed !

System Block



Presentation

Presentation

Software used during design, testing and at this presentation :

Data acquisition plug-ins from IRACE DCS

PCI driver

PCI test program

(R/W to Back-End, Formation of packets)

All made by J.Stegmeier

Presentation

- Double Correlated Readout
  - Setting of Integration Time
  - Change of Reset Bias
- Uncorrelated Readout
  - Setting of Integration Time
  - Simulator
- CCD Readout
- Noise of Video Channels
- Noise of a Clock Line at Video Channel Input