ELT AO WFS
Possible Developments

Mark Downing, D. Baade, Johann Kolb, E. Marchett, O. Iwert
European Southern Observatory ESO (http://www.eso.org)

ESO Nov 2007

Talk Overview

- What detectors are required for ELT AO WFS?
- Specification highlights:
  - ⇨ LGS
  - ⇨ NGC
- Possible LGS Solutions
- Possible NGS Solutions
- Development Plan/Schedule
- Summary

What detectors are required?

- Two types of detectors have been identified:
  - ⇨ LGS WFS detector: very large pixel format to sample spot elongation, high frame rate (700 Hz), and low noise (<3e).
  - ⇨ XAO WFS detector: for a pyramid WFS, 256^2 pixels are sufficient, but extremely high frame rate (3 to 4 kHz) and very low noise (~1 e).
- Assumed 5.5 years to develop (2008-2013) thus must be based on almost available technology
- Detector requirements differ sufficiently to believe separate development are required
- Concentrated so far on LGS WFS detector
  - ⇨ as thought to be the most challenging and
  - ⇨ Critical for the success of the ELT.

⇨ **Highest priority for ESO**

LGS Specifications highlights

Current LGS WFS baselines:

- Up to 6 Sodium LGSs (= 589 nm)
- Spatial sampling of 84 x 84 sub-apertures (goal 100 x 100)
- Sample the spot elongation by 20 x 20 pixels per sub-aperture
- Large pixels 24-50um, small full well < 4000e
- 100% fill for maximum flexibility
- High temporal sampling of 7oo Hz
- High QE > 90%
- Low RON < 3e- (goal <1 e-), DC < 0.5e/pix/frame
- Good spatial PSF of 0.8pixel
- Handle pulsed lasers (several pulses per int. time)
  - ⇨ Non-destructive electronic shuttering
  - ⇨ Noiseless addition of charge from laser pulses
- Ease of use/compact size:
  - ⇨ Integrated Read-Out electronics
  - ⇨ Simple (if possible digital) industry std interface
  - ⇨ Goal: data compress by performing centroid on-chip
  - ⇨ Peltier cooling
- Goal: Extension to first light NGS WF Sensing

XAO Specifications highlights

Current XAO WFS baselines:

- XAO Pyramid wavefront sensing
- Spatial sampling of 200 x 200 sub-apertures
- 4 quadrant detection (separate detectors) of 200x200 pixels
- Large pixels 24-50um, small full well < 4000e
- Very High temporal sampling of 3-4 kHz
- High QE > 90% (450-1000nm) especially into the RED
- Low RON < 1e-, DC << 0.1e/pix/frame
- Good spatial of PSF 0.8pixel
- Ease of use/compact size:
  - ⇨Integrated Read-Out electronics
  - ⇨Simple interface
  - ⇨Peltier cooling

Talk Overview

- What detectors are required?
- Specification highlights:
  - LGS
  - NGC
- Possible LGS Solutions
- Possible NGS Solutions
- Development Plan/Schedule
- Summary

Performed Design Studies to Get Answers

EUROPEAN SOUTHERN OBSERVATORY

Organisation Européenne pour des Recherches Astronomiques dans l'Hémisphère Austral
Europäische Organisation für astronomische Forschung in der südlichen Hemisphäre

VLT PROGRAMME

TELESCOPE SYSTEMS DIVISION

ELT Visible Adaptive Optics WFS Detector
Conceptual Design Study

Statement of Work

EUROPEAN SOUTHERN OBSERVATORY

Organisation Européenne pour des Recherches Astronomiques dans l'Hémisphère Austral
Europäische Organisation für astronomische Forschung in der südlichen Hemisphäre

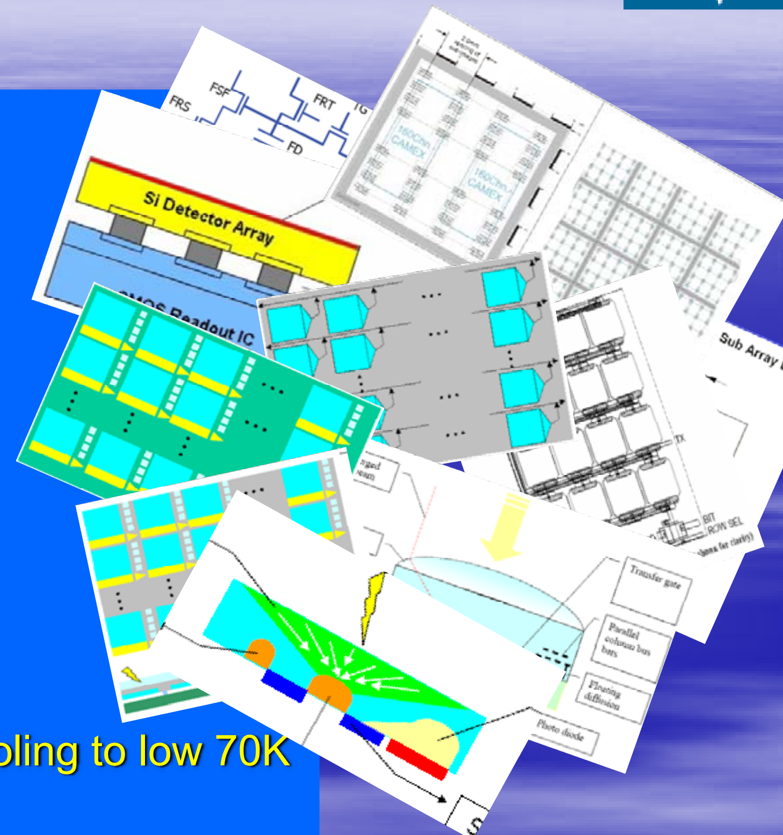
VLT PROGRAMME

TELESCOPE SYSTEMS DIVISION

ELT Visible Adaptive Optics WFS Detector
Technical Specifications

Milestones	Date (months)	Deliverables
Milestone 1: Start contract	To	Contract signature and Kick-Off Meeting Minutes of KO meeting
Milestone 2: Straw-Man Design Report	To + 2	Report one week before meeting Straw-man Design Report and Progress Meeting
Milestone 3: Design Review	To + 6	Detector Conceptual Design Study Report Review Meeting 4 weeks later Minutes of Design Review Meeting

Lots of options studied but discarded!



Discarded:

- HyViSi
- 3-D integrated FPA (MIT/LL)
- CCD/CMOS with charge detection in CMOS
- CCD/CMOS with charge detection in CCD
- CMOS Mosaic
- CCD Mosaic
- CMOS/CMOS hybrid
- pnCCDs Mosaic

Reasons:

⇨ Not able to reach read noise and/or require cooling to low 70K temperatures

⇨ Serious trades between parameters; noise, power dissipation, latency and read out speed

⇨ Too complex and/or manufacturability issues

⇨ Technology immature.

	Front Side	Hybrid	3D	Backside
QE	red	green	green	green
Dark Current	green	red	green	yellow
Noise	green	yellow	green	green
100% Operability	green	red	green	green
Size/Stitching	green	green	red	green
VLSI capability	green	green	red	green
Manufacturability	green	green	red	yellow

red: may not achieve requirements
yellow: feasible
green: demonstrated

The Survivors

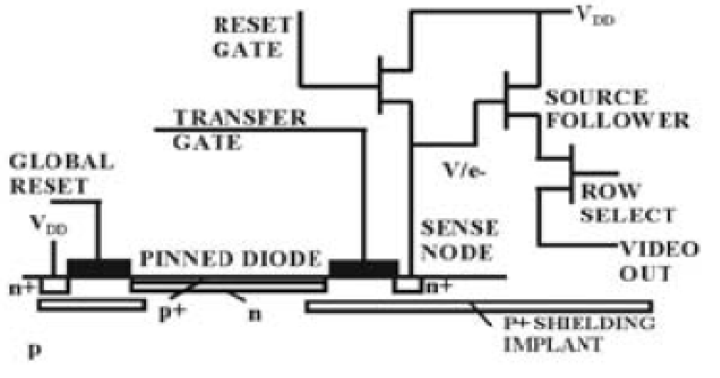
- Monolithic CMOS
  - ⇨ Front-Side Illuminated (FSI)
  - ⇨ Back-side Illuminated (BSI)
- Orthogonal Transfer CCD
- APD/CMOS Hybrid

Note that ESO has signed NDA agreements and is limited to amount of detail that can be shown.

Monolithic CMOS

Use novel pixel designs that:

- Pin the photodiode to reduce dark current to make just below zero operation possible
- Build a CCD into the pixel to
  - ⇨ Noiselessly sample multiple laser pulses,
  - ⇨ Decouple the photodiode capacitance for high conversion gain (and low noise) and good linearity
  - ⇨ enables true DCS
- Build from large transistors to reduce occurrence of RTS noise
- Do DCS within the pixel to circumvent trade between read out speed and signal analog processing time.
- Do on-chip digitization for simple digital interface
- Do LVDS for glueless interface to FPGA (e.g. Xilinx)

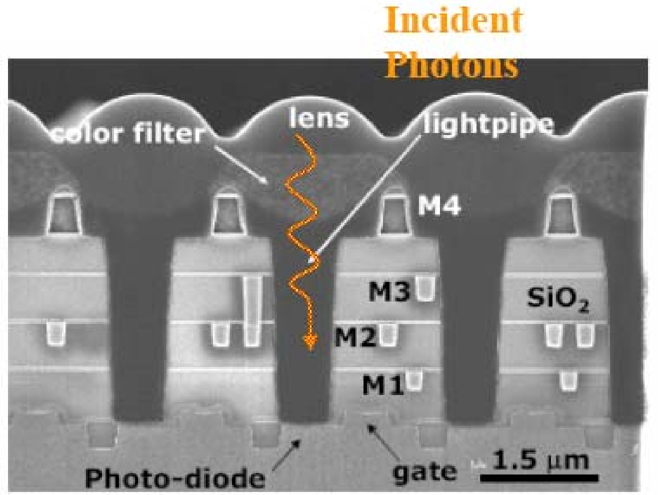


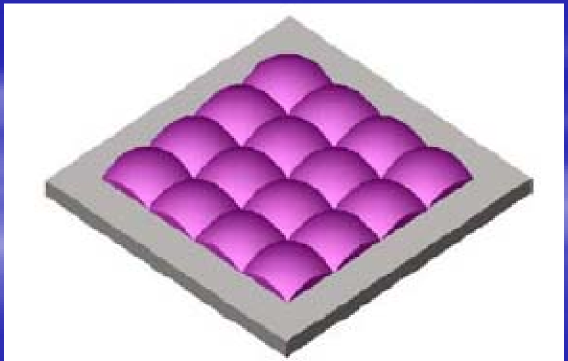
PDD 5T Pixel

Example only

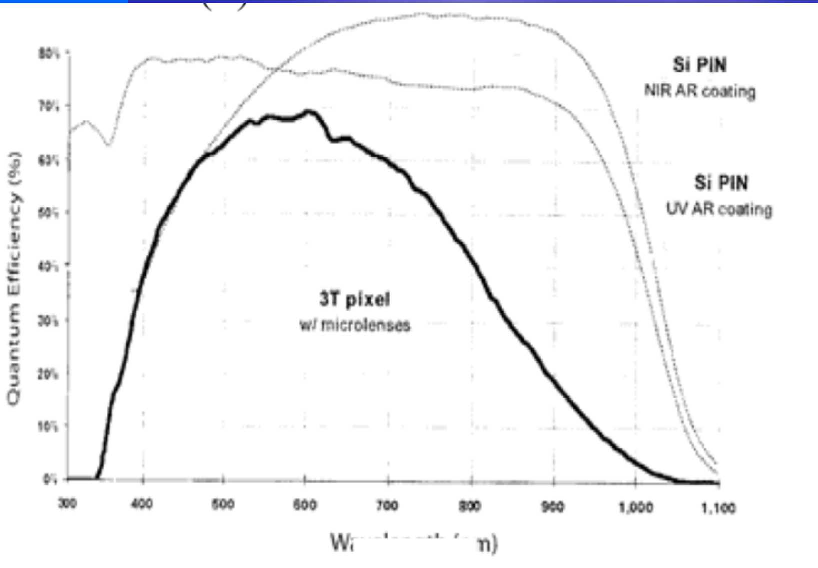
FSI Monolithic CMOS

- Use advanced techniques to improve QE:
  - ⇨ Gapless micro lenses (100% pixel fill) to overcome problem of structures inside the pixel
  - ⇨ Optical light pipes through interlayer dielectrics
- Low risk first step with current technology
- Drawbacks are behavior of the microlens array, but their quality is improving fast and QE of ~ 80% estimated.



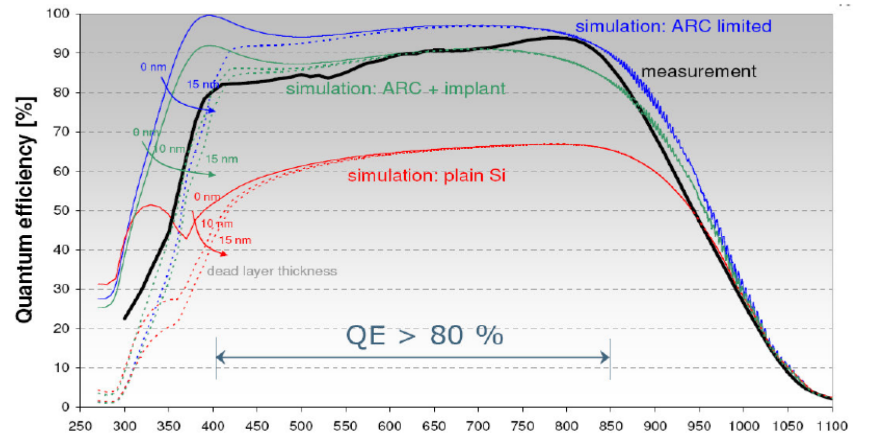


Gapless microlenses

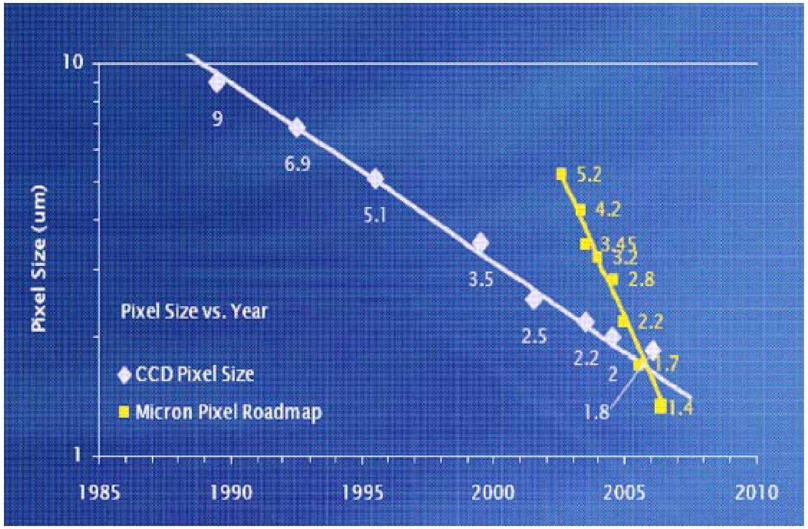


BSI Monolithic CMOS

- Although technology is very new specifications can almost already be met today
  - ⇨ QE> 80% from 450 –850 nm
  - ⇨ Dark current - 14pA/cm2
- BSI CMOS will become the technology for Mobile Phone Cameras. At pixel size of <1.2um backside illumination will be cheaper
  - ⇨ Compared to light piping or buried u-lens
  - ⇨ Many CIS foundries/fabs are working on backside illumination
- We could benefit from this technology development

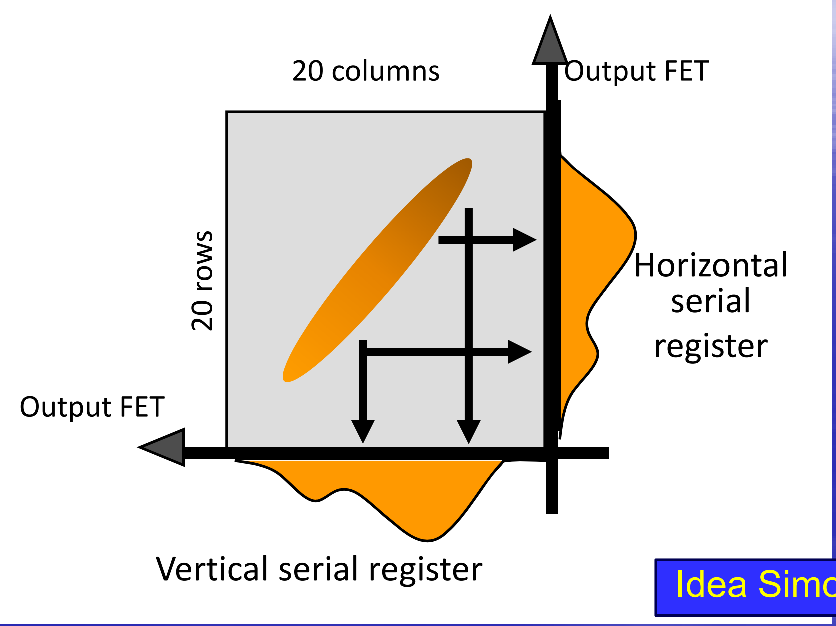


[Bogaerts] J. Bogaerts, K. De Munck, P. De Moor, D. Sabuncuoglu Tezcan, I. Ficai Veltroni, G. Lepage, C. Van Hoff, "Radiometric Performance Enhancement of Hybrid and Monolithic Backside Illuminated CMOS APS for Space –borne Imaging", 2007 International Image Sensor Workshop



Pixel Size Roadmap (from Micron Technologies)

Orthogonal Transfer CCD



Idea Simon Tulloch

- Read out X/Y profile rather than the whole image.
- After each half integration time transfer and bin charge in X or Y.
- Data compression of ~ 10 (20pixels/2 samples of X and Y).
- Add integral pixel electronic shutter:
  - ⇨ shutter drain competes with pixel electrode for collection of charge
- Use electron multiplication for output; < 1e RON

Orthogonal Transfer CCD Considerations

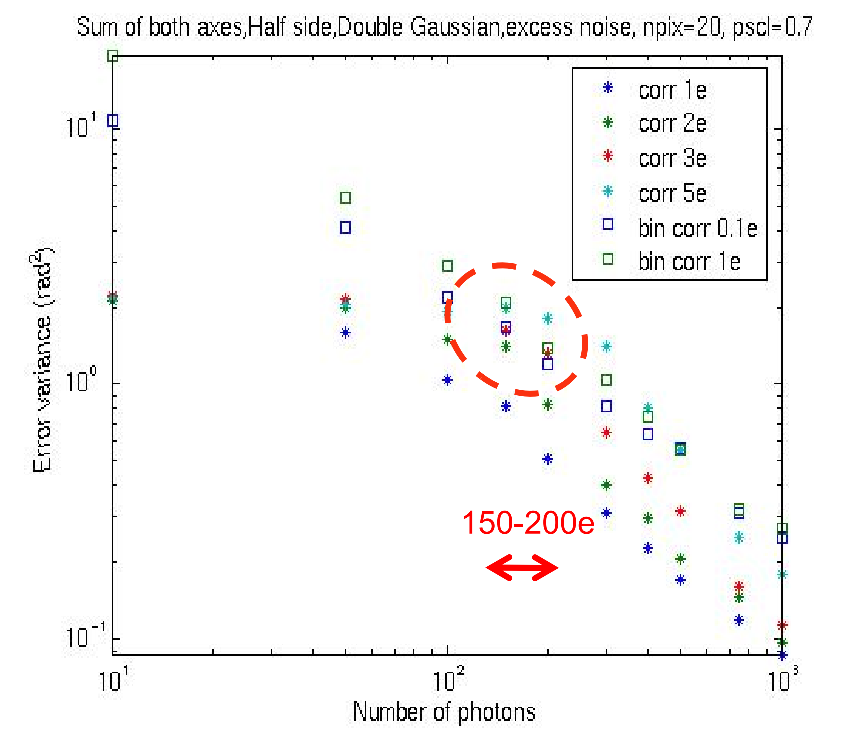
Pros:

- ✓ 10 times data compression
- ✓ reduce amplifier count to comparative manageable number
- ✓ Signal is summed (binned) thus improvement in S/N; more signal per binned pixel but same RON.
- ✓ Less data and in 1D form so less processing in the RTC

Cons:

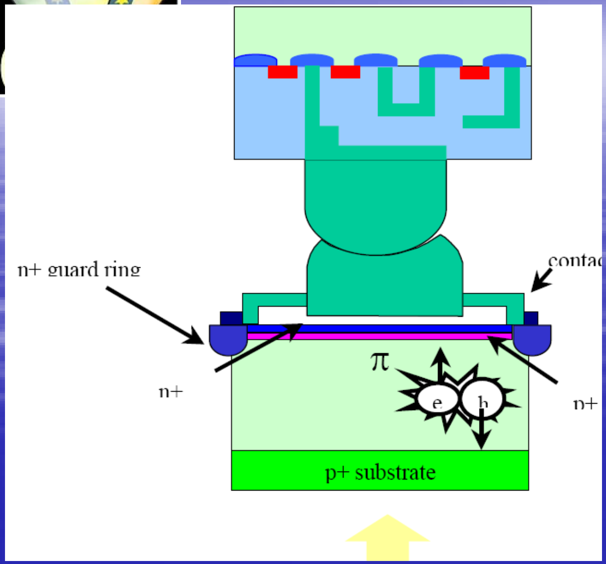
- ✗ Half of the light is effectively lost since the frame rate must be doubled to 1.4KHz
- ✗ Excess noise → effective QE is halved
- ✗ Binning adds dark current of pixels
- ✗ Sky noise added to LGS image through the binning process
- ✗ Some loss of structural information in the LGS image
- ✗ Less flexible as fill factor < 100%
- ✗ Large number of electron multiplication outputs still need to be demonstrated

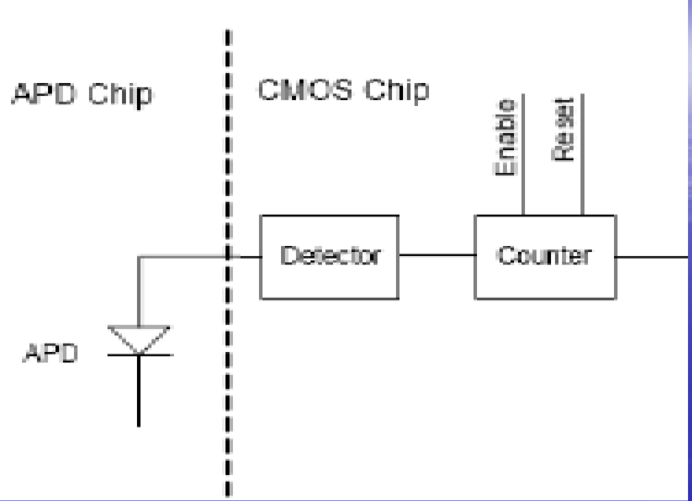
Orthogonal Transfer CCD Simulations

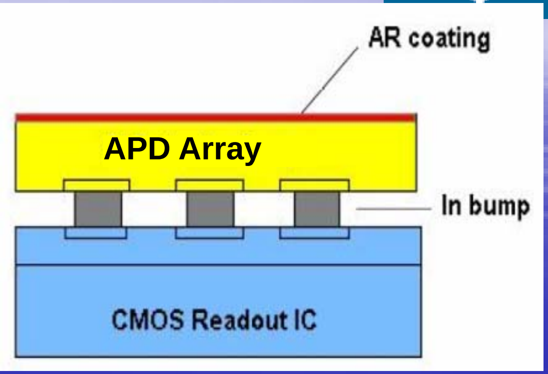


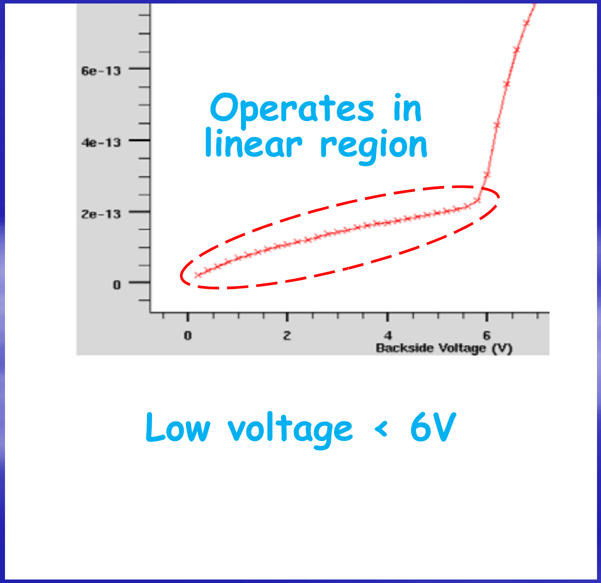
- Early simulation results:
  - ⇨ At expected LGS signal ~ 150-200e per subaperture, 0.1e RON orthogonal CCD performs as good as a 3e RON conventional detector.
- Additional work:
  - ⇨ Optimize the centroid computation.
  - ⇨ Simulate full system rather than consider only the sub-aperture.
- **Could be a good backup plan.**

APD/CMOS Hybrid









- Backthinned Avalanche Photo Diode Array hybridized to a CMOS (0.18um) detection/thresholder/counter read out.
- Modest APD gain of ~ 100-200, low voltage < 6V
- Photon counter within the pixel by thresholding single events and incrementing a counter.
- Simple shuttering by resetting and enabling the counter.
- Simple digital (e.g. LVDS) output interface
- Low pin connections: Master clock, 3V3 power/gnd, APD bias (-10V), and shutter/read out synchronizing signals.

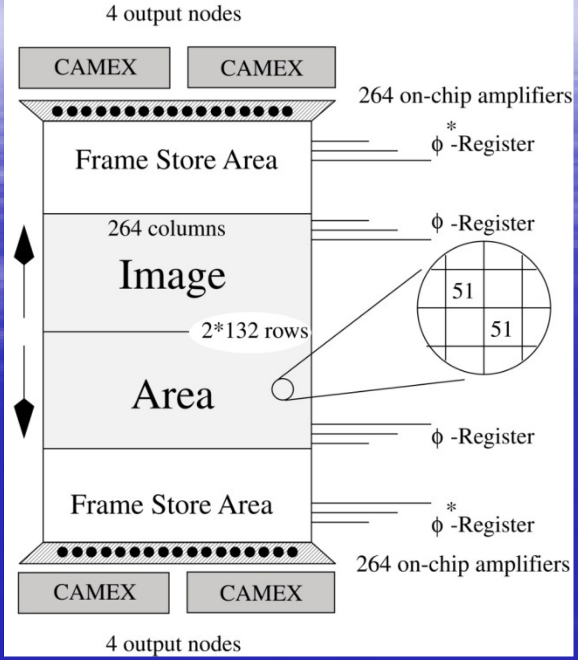
Centroid Processor Off-Chip

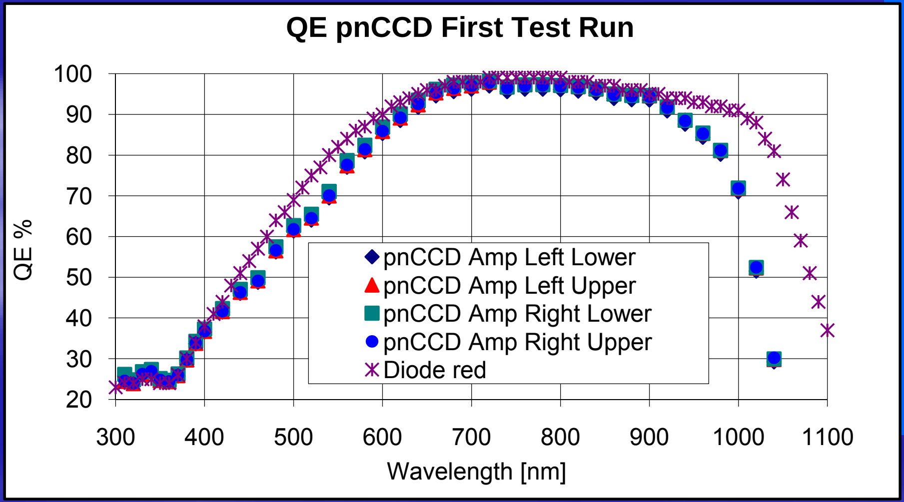
- All design studies recommended to do centroiding off-chip.
  - ⇨ Power dissipation, noise cross-talk and too high risk quoted as main reasons
- FPGAs identified as good design platform with minimal glue logic to sensor.
- Requirements are challenging:
  - ⇨ **125GFlops (19.6Mflops per sub-aperture), the total memory 102MB (16kB per sub-aperture), and the external data bandwidth 170Mbyte/s.**
    - ✓ 20 words (40 bytes) of memory per pixel
    - ✓ 70 integer/floating point operations per pixel per read out frame
    - ✓ Receive 4 floating point/integer parameters (e.g. pixel weighting, sodium layer profile information) per pixel every second
    - ✓ Transmit X and Y centroid, a measure of the image sharpness, and the intensity $\Sigma_x \Sigma_y I_{x,y}$ per subaperture per read out frame
    - ✓ Transmit raw 10 times a second for model updating and diagnostic purposes.
    - ✓ Achieve Centroid Calculation Latency < 100µs per subaperture

Talk Overview

- What detectors are required?
- Specification highlights:
  - LGS
  - NGC
- Possible LGS Solutions
- Possible NGS Solutions
- Development Plan/Schedule/FP7 Opportunity
- Summary

Take 264x264 pnCCD





- Too small for LGS detector!
- 264x264 51um pixel
- 450um thick
- Split frame transfer
- One output amplifier per column
- Total 528 amplifiers
- 1000fps
- RON < 3e
- Integrated with CAMEX
  - Gain
  - Analog DCS signal processing
  - Multiplexing of 132 channel to 1 output

And Add APD Output

- See talk “AA-pnCCD detector development plan - Henk Spruit”
- Question: Can the AA-pnCCD be sped up to 3kfps?

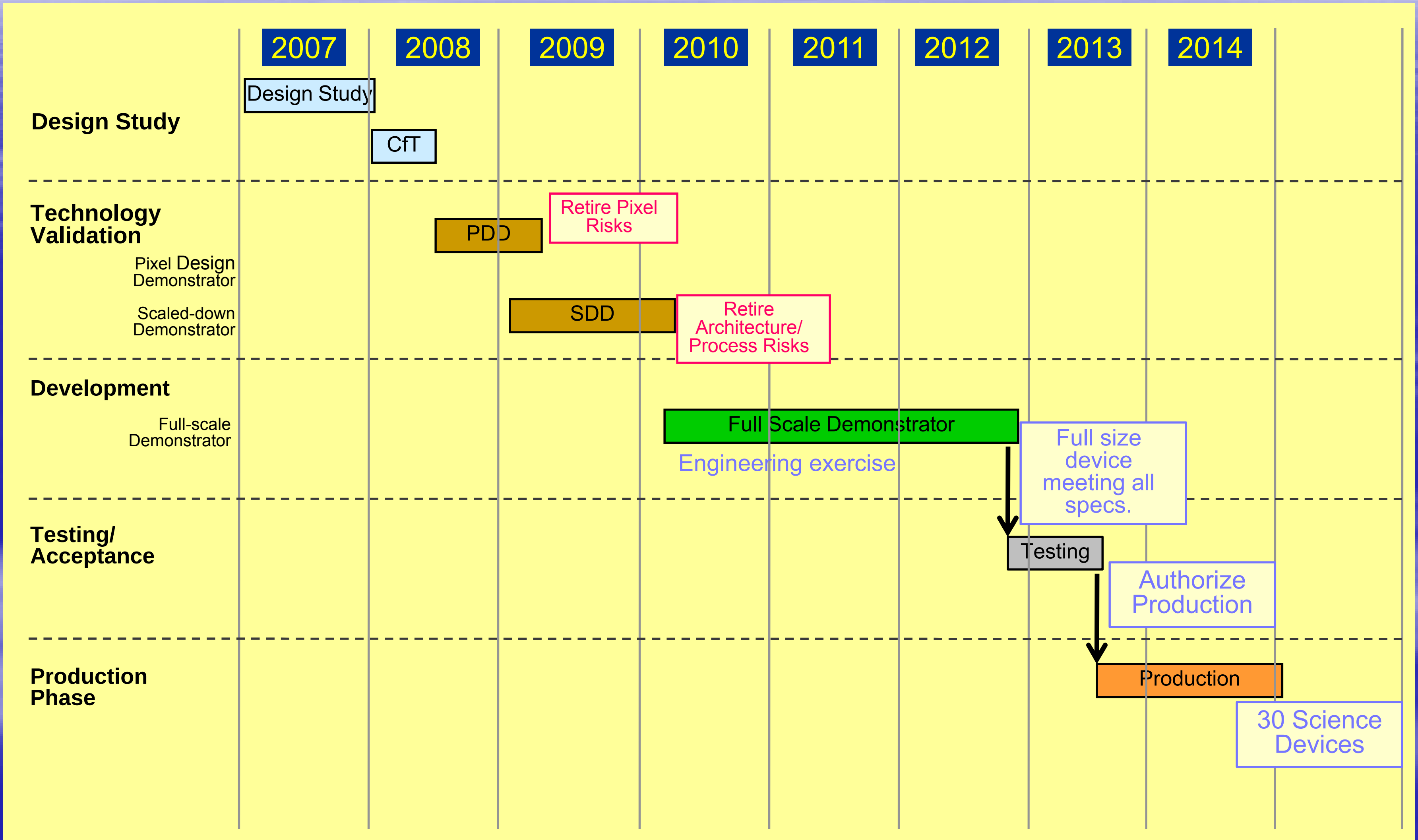
Talk Overview

- What detectors are required?
- Specification highlights:
  - LGS
  - NGC
- Possible LGS Solutions
- Possible NGS Solutions
- Development Plan/Schedule
- Summary

LGS Development Plan

- Most of the solutions for the LGS detector are almost there separately but will require a technology validation phase where existing components are put together and some interesting new concepts/ideas are explored.
- Technology validation phase will consist of two steps (biggest risks first) :
  - ⇨ Pixel Design Demonstrator (PD) where several pixel designs and geometries are tested to optimize read noise, high speed operation, shutter extinction, APD gain, bump bond yield etc.
  - ⇨ Scaled-Down Demonstrator (SDD) where chip architecture is proved. A device will be developed that functions similar (with ADCs, multiplexing logic and output LVDS interface) to the final unit but of a smaller size (and lower cost).
- Full Scale Demonstrator
  - ⇨ Manufacture full size device (identical to final) meeting all specifications
- Testing and Acceptance
  - ⇨ Verify performance and give the go ahead to manufacture the final devices
- Production Phase
  - ⇨ Up to 30 final devices are manufactured

Schedule



2007
2008
2009
2010
2011
2012
2013
2014
Design Study
Design Study
CfT
Technology Validation
Pixel Design Demonstrator
Scaled-down Demonstrator
PDD
Retire Pixel Risks
SDD
Retire Architecture/ Process Risks
Development
Full-scale Demonstrator
Full Scale Demonstrator
Engineering exercise
Full size device meeting all specs.
Testing/ Acceptance
Testing
Authorize Production
Production Phase
Production
30 Science Devices

Summary

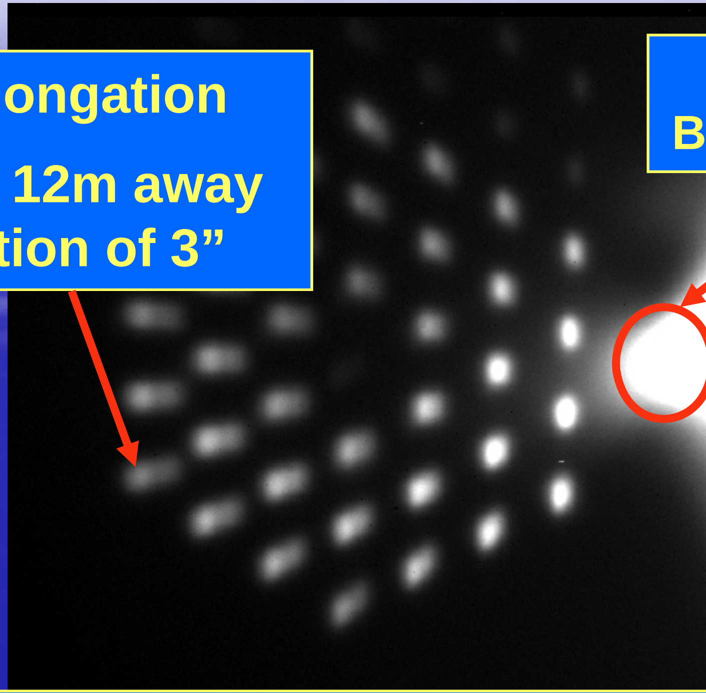
- Two types of AO WFS detectors identified for ELT:
  - ⇨ LGS WFS detector: 1600x1600pixels, 700 frame/sec, and low noise (<3e).
  - ⇨ XAO WFS detector: 255x256pixels, 3-4 kframe/sec, and very low noise (~1 e)
- Requirements for LGS detector are most challenging but constituents of several solutions almost exist:
  - ⇨ Monolithic CMOS
  - ⇨ APD/CMOS Hybrid
  - ⇨ Orthogonal Transfer CCD
- Development plan broken down into several phases will allow progressive retirement of risk at the earliest opportunity (largest ones first) and guarantee final success.

END
Thanks

LGS based AO challenges on ELT

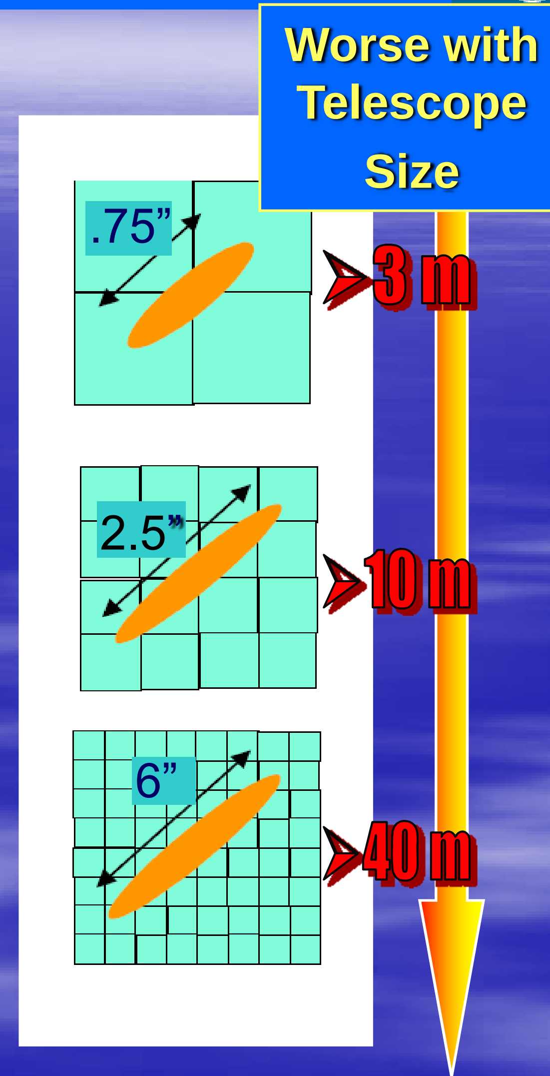
Spot Elongation

aperture 12m away elongation of 3”



Rayleigh Backscatter

Laser Launch Site



Probably need ~ 20x20 pixels for each spot to properly sample the elongation.

- Large amount of pixels for spot elongation issue
- With pulsed laser: electronic shutter (sodium spot only)