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Installation Report UVES Red CCD upgrade

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Issue/Revision	Date	Section/Page Affected	by	Reason
1	Jul/2009	All	NHA	First draft
2	Jan/2010	All	NHA	Changes in all sections
2.5	Apr/2010	All	NHA	Images scaled to reduce document size

List of Abbreviation

ADC	Analog to Digital Converter
ADU	Analog to Digital Unit
ATM	Asynchronous Transfer Mode
BOB	Broker for Observation Blocks
CCD	Charge Coupled Device
CFC	Continuous Flow Cryostat
DSP	Digital Signal Processor
EMI	Electromagnetic Immunity
EPER	Extended Pixel Edge Response
FIERA	Fast Imager Electronic Readout Assembly
Gbps	Gigabit/second
IC-LCU	Instrument Control LCU
ICS	Instrument Control System
kps	kilopixel/port/second
LAN	Local Area Network
LCU	Local Control Unit
Mps	Megapixel/port/second
MTBF	Mean Time Between Failures
MIDAS	Image processing software package
ODT	Optical Detector Team
PRISM	Image processing software package
TBD	To Be Defined
WS	Workstation

Table of Contents

Introduction

This documents reports on the upgrade of the UVES RED detector system, in order to replace the MIT chip CCID20-W720, code name Nigel by the MIT 40um thick, high resistivity, deep depletion back illuminated chip CCID20-4-10-2, code name ZEUS.

The main goals of the upgrade were to take advantage of the better QE of Zeus in the 600nm to 1um region and its improved fringing behavior in the red part of the spectrum and also benefit from the improved cosmetic of Zeus with respect to Nigel

To perform the upgrade, the RED UVES cryostat and DFE electronics plus cables were shipped to Garching.

The detector assembly was removed and installed in a new detector head fitted with a flat window to allow the measuring of the QE in the ODT new test bench.

Measurement were done to determine the relative position of the Nigel MIT chip with respect to the EEV CCD. These values were used as a reference to install the new chip.

New QE measurements were performed on the MIT chip to be replaced (Nigel) and these results are used in this document to compare the QE of Zeus and Nigel. The old QE values for Nigel had been taken long time ago and with a different CCD test bench, so it was decided to use the same setup for the QE measurements.

Information on the mechanical and electrical characteristic of the MIT chip can be found in the internal ODT web pages, at *http://www.eso.org/intra/org/ins/optdet/Testbench/MIT/MITLL_Datasheet.pdf*

Performance summary tables

Table 1: Summary of Performance

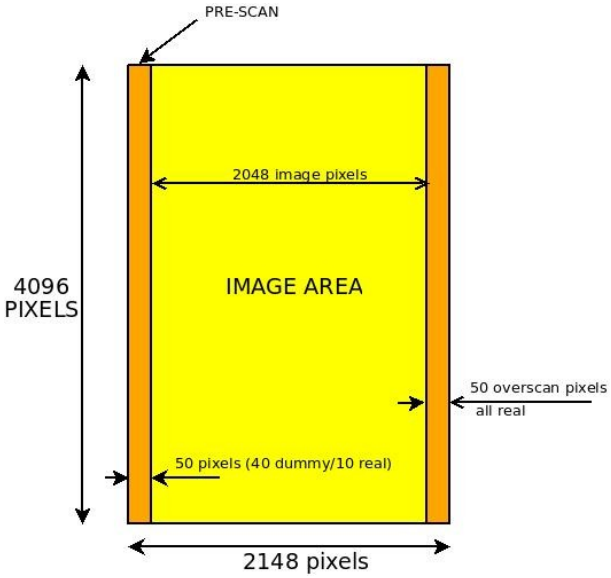
Parameter	Specification	Comments
Device	Zeus	
Type number	CCI20	Backside, 40um thickness, Single layer AR
Serial number	04/10/02	
Pixel size	15um	
Number of image Pixels	2048x4096	
Cosmetic quality	Cosmetically clean 2 bad columns	#1@1253,917 affects 3178 pixels #2@1973,3173 affects 922 pixels
Cosmic hit event rate (Paranal)	1144 hits/cm2/hr	
Vertical CTE	0.999999	
Horizontal CTE	0.9999967	
Linearity	< +/- 0.5% peak to peak	
Dark Current	< 0.9 e/pix/hr	
QE @ 500 nm	74 %	
QE @ 600 nm	82 %	
QE @ 700 nm	87 %	
QE @ 800 nm	85 %	
QE @ 900 nm	64 %	
QE @ 1000 nm	19%	

CCD dimensions and data format

No changes have been implemented with respect to the CCD dimensions and data format.

This chip has 10 pre-scan pixels, but in order to read it in synchronism with the EEV chip, which has 50 prescan pixels, 40 dummy pixels are added at the beginning of the image. In the vertical direction, there are 4096 pixels, with no over-scan implemented in the readout modes.

The following image illustrate the chip format.



UVES RED Readout Modes

The offered readout modes are:

50khz,2x2,hg

50khz,2x3,hg

225khz,1x1,lg

225khz,2x2,lg

625khz,1x1,lg

Note: **lg** means Low Gain and **hg** means High Gain

Cryogenic parameters

CCD temperatures

Both CCDs on the UVES RED cryostat are operated at the same temperature. The cryostat is connected to a Continuous Flow Cryostat which keeps control of the cold plate temperature through the activation of an electromagnetic valve that circulates LN2 on the cryostat. The cryostat cold plate is thermally connected through a cold finger to the detectors mounting plate which have a two heaters controlled by PULPO to have a fine control of the CCD temperature.

Telemetry and alarms

Cryostat Cold Plate set point	-190 C
Cryostat air heater set point	0 C
CCDs temperature set point (PULPO)	135 K (-138.15 C)
Alarm trigger value on PULPO	137 K (-136.15 C)
Alarm trigger value for cold plate on CFC	-195 C
Alarm trigger value for air heater on CFC	10 C

FIERA detector head electronics and hardware setup

CCD operating voltages

The file volttable.def was modified to have the same values that have been used by ZEUS during it's operation on EMMI RED. During the installation in Paranal, we discovered that some spurious charge was generated during the parallel transfer of the charge. To eliminate this problem the negative parallel voltage swing was reduced to -5.5V instead the original 6.0V

The contents of the voltage definition file follows:

$INSROOT/SYSTEM/COMMON/CONFIGFILES/.../volttable.def

```
#
# "@(#) $Id: volttable.def,v 1.20 2009/07/13 18:56:00 vltsccm Exp $"
#
#############################################################################
#Author:       Reinhold Dorn
#CAMERA:        UVES RED   ( Mosaic 1 EEV CCD-44 and 1 MITLL CCID-20
#Purpose:      This is the global voltage definition table micro sequences
#              European Southern Observatory (ESO)
#Date:         15.06.98
#
#Modified:      Nicolas Haddad
#Reason:        MIT chip changed on May 2009. Voltages fro ZEUS applied
#Date:          28.06.2009
#############################################################################
#  GOBAL VOLTAGE DEFINITION TABLE
#
# This table defines the voltages which will be applied to peripherals
# at initialisation time. It also defines the high and low limits which may
# be set for these voltages
#############################################################################
# BRD_ID  PERIPH_ID            LOW    HIGH    TOLERANCE     INIT_VAL
#
# Anabias voltages are in 0.001 volts
#
#############################################################################
#  BIASBRD 0 is for the EEV CCD-44 in the mosaic
#############################################################################
# BRD_ID  PERIPH_ID            LOW    HIGH    TOLERANCE     INIT_VAL

# CONNECTOR P0 - A

BRD_ANABIAS0 ANB_PRESET_VOLT_A       -3500   -1000   10000        -3500 #OG1R
BRD_ANABIAS0 ANB_PRESET_VOLT_B       -2500   -1000   10000        -2500 #OG2R
BRD_ANABIAS0 ANB_PRESET_VOLT_C        2000   25000   10000        23000 #ODR
BRD_ANABIAS0 ANB_PRESET_VOLT_D        2000   15000   10000        12000 #RDR
BRD_ANABIAS0 ANB_PRESET_VOLT_E        2000   25000   10000        24000 #JDR
BRD_ANABIAS0 ANB_PRESET_VOLT_F           0       0       0            0 #not used
BRD_ANABIAS0 ANB_PRESET_VOLT_G           0       0       0            0 #not used
BRD_ANABIAS0 ANB_PRESET_VOLT_H           0       0       0            0 #not used

# CONNECTOR PO - B

BRD_ANABIAS0 ANB_PRESET_VOLT_I       -3500  -1000    10000        -3500 #OG1L
BRD_ANABIAS0 ANB_PRESET_VOLT_J       -2500  -1000    10000        -2500 #OG2L
BRD_ANABIAS0 ANB_PRESET_VOLT_K        2000  25000   10000        23000 #ODL
```

```
BRD_ANABIAS0 ANB_PRESET_VOLT_L        2000   15000    10000         12000 #RDL
BRD_ANABIAS0 ANB_PRESET_VOLT_M        2000   25000    10000         24000 #JDL
BRD_ANABIAS0 ANB_PRESET_VOLT_N           0       0        0             0 #not used
BRD_ANABIAS0 ANB_PRESET_VOLT_O        2000   19000    10000         18000 #DDLR
BRD_ANABIAS0 ANB_PRESET_VOLT_P           0       0        0             0 #not used

###############################################################################
#  BIASBRD 1 is for the MIT/LL CCID in the mosaic
###############################################################################
# BRD_ID  PERIPH_ID            LOW    HIGH    TOLERANCE     INIT_VAL

# CONNECTOR PO - C
BRD_ANABIAS1 ANB_PRESET_VOLT_A        5000      20000    10000         20000 #OD-A (NHA May 09)
BRD_ANABIAS1 ANB_PRESET_VOLT_B           0          0    10000             0 #OG-A
BRD_ANABIAS1 ANB_PRESET_VOLT_C        5000      15000    10000         12500 #RD-A
BRD_ANABIAS1 ANB_PRESET_VOLT_D        5000      13000    10000         13000 #SCP-A (NHA May 09)
BRD_ANABIAS1 ANB_PRESET_VOLT_E          0       0       0             0 #not used
BRD_ANABIAS1 ANB_PRESET_VOLT_F          0       0       0             0 #not used
BRD_ANABIAS1 ANB_PRESET_VOLT_G          0       0       0             0 #not used
BRD_ANABIAS1 ANB_PRESET_VOLT_H          0       0       0             0 #not used
# CONNECTOR PO - D
BRD_ANABIAS1 ANB_PRESET_VOLT_I        5000      20000    10000         20000 #OD-B (NHA May 09)
BRD_ANABIAS1 ANB_PRESET_VOLT_J           0          0    10000             0 #OG-B
BRD_ANABIAS1 ANB_PRESET_VOLT_K        5000      15000    10000         12500 #RD-B
BRD_ANABIAS1 ANB_PRESET_VOLT_L        5000      13000    10000         13000 #SCP-B (NHA May 09)
BRD_ANABIAS1 ANB_PRESET_VOLT_M          0       0       0             0 #not used
BRD_ANABIAS1 ANB_PRESET_VOLT_N          0       0       0             0 #not used
BRD_ANABIAS1 ANB_PRESET_VOLT_O          0       0       0             0 #not used
BRD_ANABIAS1 ANB_PRESET_VOLT_P          0       0       0             0 #not used

#The anabias board also has an opto isolated peripheral
BRD_ANABIAS1 ANB_OPTOOUT      0       32767   4               255
#
###############################################################################
# Clock driver rail voltages are in 0.001 volts
#
###############################################################################
#CLOCKDRIVER BOARD 0 is for the EEV CCD44 in the mosaic
###############################################################################
#
#
# BRD_ID       PERIPH_ID         LOW         HIGH      TOLERANCE    INIT_VAL
#
#   CONNECTOR PO-A
#
BRD_CLKDRV0 CLKDRV_DAC0_LO      -5000       -5000      1000        -5000 #SWL
BRD_CLKDRV0 CLKDRV_DAC0_HI       5000        5000      1000         5000
BRD_CLKDRV0 CLKDRV_DAC1_LO      -5000       -5000      1000        -5000 #SWR
BRD_CLKDRV0 CLKDRV_DAC1_HI       5000        5000      1000         5000
BRD_CLKDRV0 CLKDRV_DAC2_LO      -5000       -5000      1000        -5000 #RF3
BRD_CLKDRV0 CLKDRV_DAC2_HI       5000        5000      1000         5000
BRD_CLKDRV0 CLKDRV_DAC3_LO      -5000       -5000      1000        -5000 #RF2L
BRD_CLKDRV0 CLKDRV_DAC3_HI       5000        5000      1000         5000
BRD_CLKDRV0 CLKDRV_DAC4_LO      -5000       -5000      1000        -5000 #RF1L
BRD_CLKDRV0 CLKDRV_DAC4_HI       5000        5000      1000         5000
BRD_CLKDRV0 CLKDRV_DAC5_LO      -5000       -5000      1000        -5000 #RF2R
BRD_CLKDRV0 CLKDRV_DAC5_HI       5000        5000      1000         5000
BRD_CLKDRV0 CLKDRV_DAC6_LO      -5000       -5000      1000        -5000 #RF1R
BRD_CLKDRV0 CLKDRV_DAC6_HI       5000        5000      1000         5000
BRD_CLKDRV0 CLKDRV_DAC7_LO      -6000       -6000      1000        -6000 #DG
BRD_CLKDRV0 CLKDRV_DAC7_HI       6000        6000      1000         6000
#
#     CONNECTOR PO-B
#
BRD_CLKDRV0 CLKDRV_DAC8_LO     -12000       -4000      1000        -8000 #IF1
BRD_CLKDRV0 CLKDRV_DAC8_HI      -2000        3000      1000         2000
BRD_CLKDRV0 CLKDRV_DAC9_LO     -12000       -4000      1000        -8000 #IF2
BRD_CLKDRV0 CLKDRV_DAC9_HI      -2000        3000      1000         2000
BRD_CLKDRV0 CLKDRV_DAC10_LO    -12000       -4000      1000        -8000 #IF3
BRD_CLKDRV0 CLKDRV_DAC10_HI     -2000        3000      1000         2000
```

```
BRD_CLKDRV0 CLKDRV_DAC11_LO    -0000      -0000     1000       -0000 #empty
BRD_CLKDRV0 CLKDRV_DAC11_HI     0000       0000     1000        0000
BRD_CLKDRV0 CLKDRV_DAC12_LO    -6000      -4000     1000       -6000 #FRL
BRD_CLKDRV0 CLKDRV_DAC12_HI     6000       8000     1000        6000
BRD_CLKDRV0 CLKDRV_DAC13_LO    -6000      -4000     1000       -6000 #FRR
BRD_CLKDRV0 CLKDRV_DAC13_HI     6000       8000     1000        6000

################################################################################
#CLOCKDRIVER BOARD 1 is for the MIT/LL  CCID-20 in the mosaic
################################################################################
#
#
# BRD_ID       PERIPH_ID        LOW        HIGH     TOLERANCE   INIT_VAL
#
#    CONNECTOR PO-C
#
BRD_CLKDRV1 CLKDRV_DAC0_LO     -5000      -5000     1000       -5000 #SWA
BRD_CLKDRV1 CLKDRV_DAC0_HI      5000       5000     1000        5000
BRD_CLKDRV1 CLKDRV_DAC1_LO     -5000      -5000     1000       -5000 #SWB
BRD_CLKDRV1 CLKDRV_DAC1_HI      5000       5000     1000        5000
BRD_CLKDRV1 CLKDRV_DAC2_LO     -3000      -3000     1000       -3000 #S3
BRD_CLKDRV1 CLKDRV_DAC2_HI      6000       6000     1000        6000
BRD_CLKDRV1 CLKDRV_DAC3_LO     -3000      -3000     1000       -3000 #S2A
BRD_CLKDRV1 CLKDRV_DAC3_HI      6000       6000     1000        6000
BRD_CLKDRV1 CLKDRV_DAC4_LO     -3000      -3000     1000       -3000 #S1A
BRD_CLKDRV1 CLKDRV_DAC4_HI      6000       6000     1000        6000
BRD_CLKDRV1 CLKDRV_DAC5_LO     -3000      -3000     1000       -3000 #S2B
BRD_CLKDRV1 CLKDRV_DAC5_HI      6000       6000     1000        6000
BRD_CLKDRV1 CLKDRV_DAC6_LO     -3000      -3000     1000       -3000 #S1B
BRD_CLKDRV1 CLKDRV_DAC6_HI      6000       6000     1000        6000
BRD_CLKDRV1 CLKDRV_DAC7_LO      0000       0000     1000        0000 #empty
BRD_CLKDRV1 CLKDRV_DAC7_HI      0000       0000     1000        0000
#
#     CONNECTOR PO-D
#
BRD_CLKDRV1 CLKDRV_DAC8_LO     -8000      -5000     1000       -5500 #P1
BRD_CLKDRV1 CLKDRV_DAC8_HI      2000       3000     1000        2000 #(NHA May 2009)
BRD_CLKDRV1 CLKDRV_DAC9_LO     -8000      -5000     1000       -5500 #P2
BRD_CLKDRV1 CLKDRV_DAC9_HI      2000       3000     1000        2000 #(NHA May 2009)
BRD_CLKDRV1 CLKDRV_DAC10_LO    -8000      -5000     1000       -5500 #P3
BRD_CLKDRV1 CLKDRV_DAC10_HI     2000       3000     1000        2000 #(NHA May 2009)
BRD_CLKDRV1 CLKDRV_DAC11_LO     0000       0000     1000        0000 #empty
BRD_CLKDRV1 CLKDRV_DAC11_HI     0000       0000     1000        0000
BRD_CLKDRV1 CLKDRV_DAC12_LO     0000       0000     1000        0000 #RGA
BRD_CLKDRV1 CLKDRV_DAC12_HI    10000      12000     1000       10000
BRD_CLKDRV1 CLKDRV_DAC13_LO     0000       0000     1000        0000 #RGB
BRD_CLKDRV1 CLKDRV_DAC13_HI    10000      12000     1000       10000


#
# Gain should be interpreted as follows
# There are two gains, gain1 is on the preamp, gain2 is on the video board.

# Gain1 =
#     3 == 1.5
#     1 == 2.25
#     0 == 3.0
#
# Gain2 =
#     0 = Minimum (2.5)
#     1 = Maximum (12.5)
#
# BRD_ID  PERIPH_ID           LOW     HIGH    TOLERANCE      INIT_VAL
BRD_VIDBRD0 VID_GAIN1_CHAN0        0        3        0               1
BRD_VIDBRD0 VID_GAIN1_CHAN1        0        3        0               1
BRD_VIDBRD0 VID_GAIN1_CHAN2        0        3        0               1
BRD_VIDBRD0 VID_GAIN1_CHAN3        0        3        0               1

BRD_VIDBRD0 VID_GAIN2_CHAN0        0        1        0               0
BRD_VIDBRD0 VID_GAIN2_CHAN1        0        1        0               0
```

```
BRD_VIDBRD0 VID_GAIN2_CHAN2       0       1       0               0
BRD_VIDBRD0 VID_GAIN2_CHAN3       0       1       0               0

BRD_VIDBRD0 VID_FILT_CHAN0        0       3       0               0
BRD_VIDBRD0 VID_FILT_CHAN1        0       3       0               0
BRD_VIDBRD0 VID_FILT_CHAN2        0       3       0               0
BRD_VIDBRD0 VID_FILT_CHAN3        0       3       0               0

BRD_VIDBRD0 VID_TESTVID_CHAN0     0       1       0               0
BRD_VIDBRD0 VID_TESTVID_CHAN1     0       1       0               0
BRD_VIDBRD0 VID_TESTVID_CHAN2     0       1       0               0
BRD_VIDBRD0 VID_TESTVID_CHAN3     0       1       0               0

#
# Video Offsets are in 0.001 volts
#
# BRD_ID  PERIPH_ID           LOW     HIGH    TOLERANCE      INIT_VAL
#


BRD_VIDBRD0 VID_OFFSET_CHAN0    0   65535    6553            32221
BRD_VIDBRD0 VID_OFFSET_CHAN1    0   65535    6553            32231
BRD_VIDBRD0 VID_OFFSET_CHAN2    0   65535    6553            849
BRD_VIDBRD0 VID_OFFSET_CHAN3    0   65535    6553            800
```

PreAmplifier Setup

The standard preamplifier board VX.X was used. The inputs channel 0 uses a 3Kohms resistor and inputs channels 1,2 and 3 are fitted with a JFET current source. The MIT chip uses channel 0 and channel 1 and the E2V chip uses channel 2 and 3. Inputs channels 0 and 1 have different load in order to investigate the noise and linearity behavior. No difference was detected, but it was decided to leave the MIT A output (used for the science modes) loaded with the standard configuration (3Kohms).

The preamplifier had the normal amplification setting, 1.5 V/V, 2.25 V/V and 3 V/V

The parameter Gain1 on the *volttable.def* and in the *gain** files defines which gain is selected from the preamplifier.

Video Board Setup

Video Board ID: 40

	MIT port A CH0	**MIT port B CH1**	**EEV port L CH2**	**EEV port R CH3**
LG resistor	R43=100ohm	R47=100 ohm	R51=120 ohm	R55=120 ohm
HG resistor	R42=56 ohm	R46=56 ohm	R50=36 ohm	R54=36 ohm
Filter0 T=150ns	C21=100pF	C25=100pF	C29=100pF	C33=100pF
Filter1 T=480ns	C22=220pF	C26=220pF	C30=220pF	C34=220pF
Filter2 T=1.5us	C23=1nF	C27=1nF	C31=1nF	C35=1nF
Filter3 T=3us	C24=2nF C374=none	C28=2nF C374=none	C32=2nF C374=none	C36=2nF C374=none
Offset range	B-C/D-E	B-C/D-E	E-F	E-F

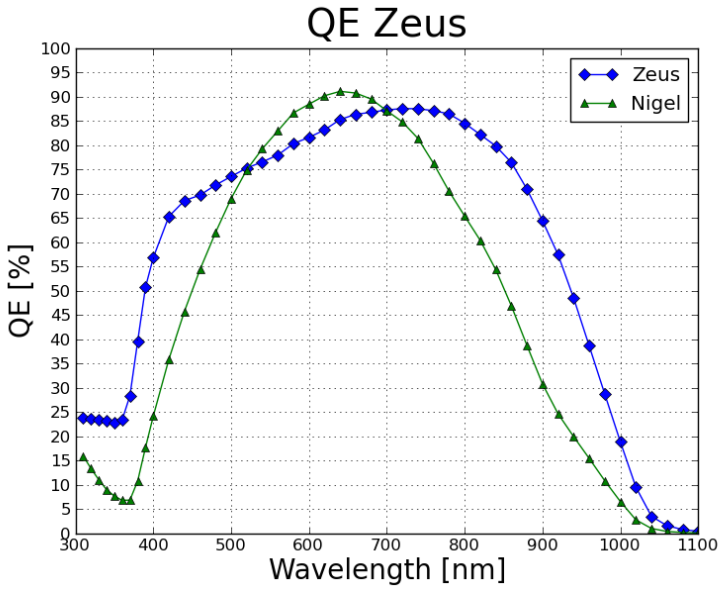
CCD system performance data

Gain and readout noise

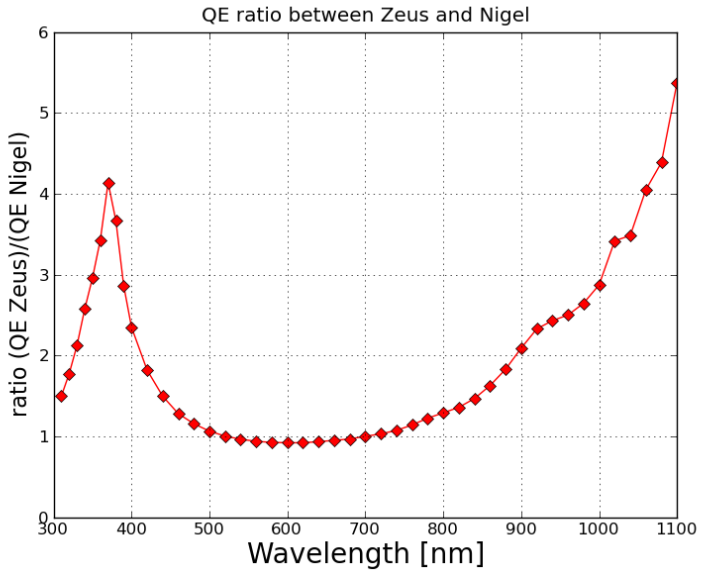
Table 1: Summary of performance of the scientific read out modes.

Clock Mode	Readout speed	Dynamic (ADC limited) [Ke/pixel]	Conversion Factor [e-/ADU]	Read Out Noise [e-]	Read Out Time [s]
2	50kps,2x2,hg	32	0.48	2.3	45
2	50kps,2x3,hg	32	0.48	2.3	31
5	225kps,1x1,lg	98	1.43	3.7	45
5	225kps,1x2,lg	98	1.43	3.7	20
9	625kps,1x1,lg	98	1.43	4.6	11

Quantum Efficiency

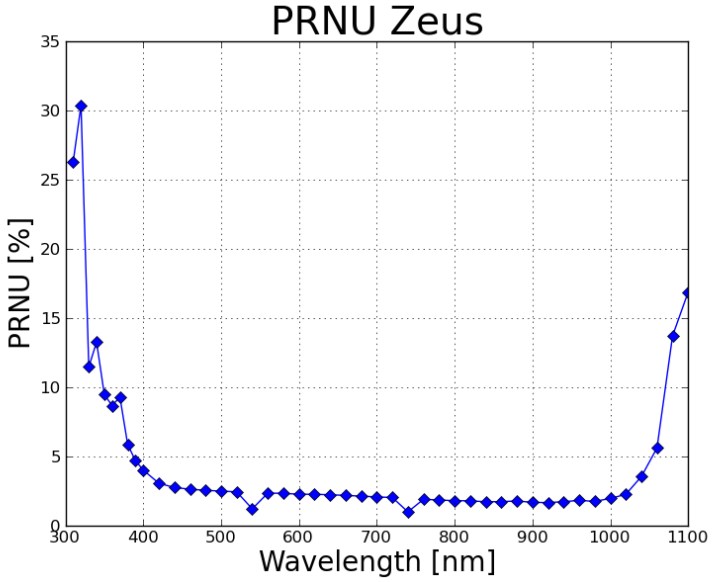


QE graph for Zeus and Nigel



QE ratio between Zeus and Nigel

The following graph show the PRNU obtained for the different wavelength during the QE testing.



PRNU for Zeus

Wavelength [nm]	QE [%]	PRNU [%]	Wavelength [nm]	QE [%]	PRNU [%]
310	23.91	26.3	680	86.79	2.12
320	23.71	30.36	700	87.27	2.06
330	23.47	11.45	720	87.55	2.02
340	23.22	13.25	740	87.51	0.98
350	22.79	9.45	760	87.12	1.89
360	23.36	8.66	780	86.45	1.84
370	28.35	9.28	800	84.53	1.79
380	39.61	5.84	820	82.19	1.78
390	50.73	4.68	840	79.84	1.71
400	56.82	4	860	76.43	1.72
420	65.31	3.05	880	70.96	1.77
440	68.57	2.74	900	64.44	1.67
460	69.71	2.62	920	57.44	1.65
480	71.78	2.54	940	48.53	1.72
500	73.55	2.48	960	38.65	1.81
520	75.28	2.43	980	28.72	1.74
540	76.55	1.2	1000	18.89	1.95
560	77.97	2.34	1020	9.54	2.25
580	80.32	2.32	1040	3.52	3.54
600	81.61	2.26	1060	1.58	5.6
620	83.14	2.25	1080	0.79	13.7
640	85.3	2.22	1100	0.43	16.86
660	86.36	2.17			

Zeus QE and Pixel Response Non Uniformity

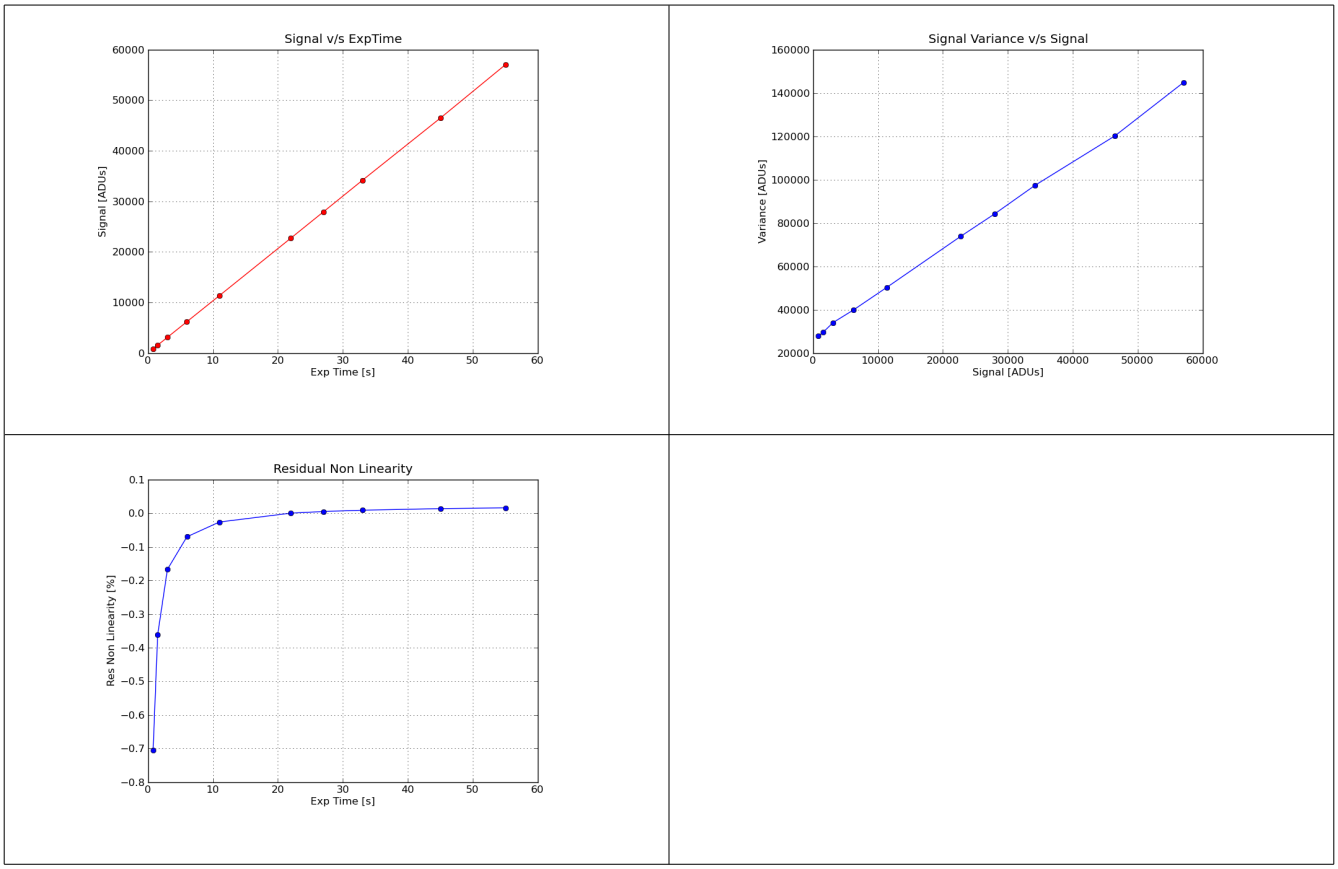
Linearity

The linearity was tested in Paranal taking a set of bias frames followed by pairs of FF of different exposure length to explore almost the complete dynamic range provided by the ADC (65535 ADUs).

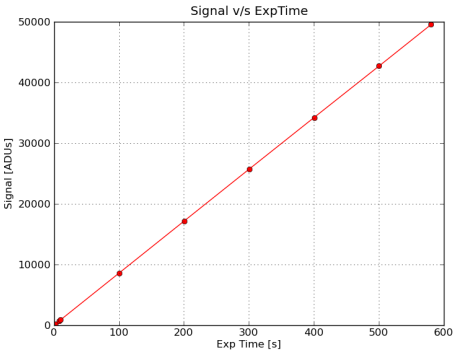
The results confirm that the CCD plus electronics residual non linearity is less than +/- 0.5 % of the and the system response is linear with respect to the exposure time.

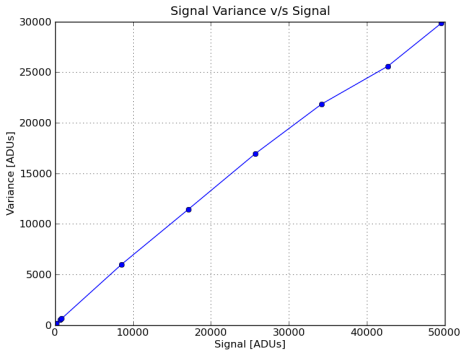
The following table and graphs shows the results for the 50Kps,2x2,hg mode.

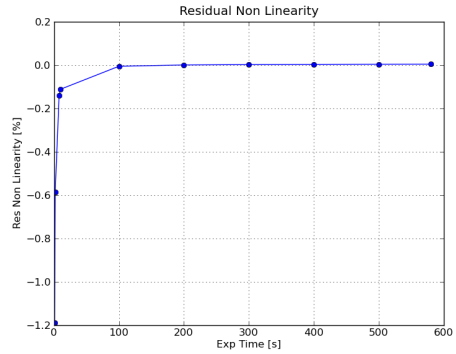
Exp Time	FF1_Mean	FF2_Mean	FF_Mean	FF2_Variance	CF
0.8	832.1	834.2	833.2	27881.5	0.48
1.5	1552.9	1555.4	1554.1	29544.2	0.48
3.0	3098.7	3103.1	3100.9	34070.4	0.47
6.0	6192.3	6193.7	6193.0	39806.4	0.48
11.0	11350.5	11350.6	11350.6	50274.6	0.48
22.0	22722.9	22727.7	22725.2	73840.9	0.48
27.0	27916.7	27913.5	27915.0	84136.1	0.49
33.0	34161.8	34151.8	34156.7	97368.0	0.49
45.0	46462.0	46469.4	46465.6	120231.0	0.49
55.0	57033.2	57000.0	57016.3	144876.0	0.48



The same linearity test was done for low gain (225Kps,1x1,low) with the following results:

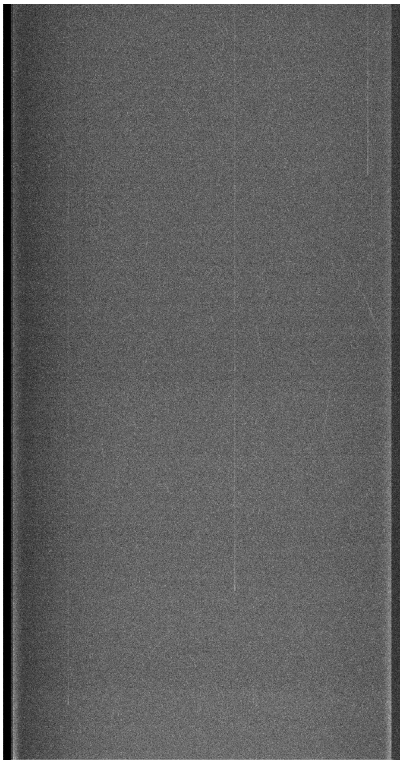




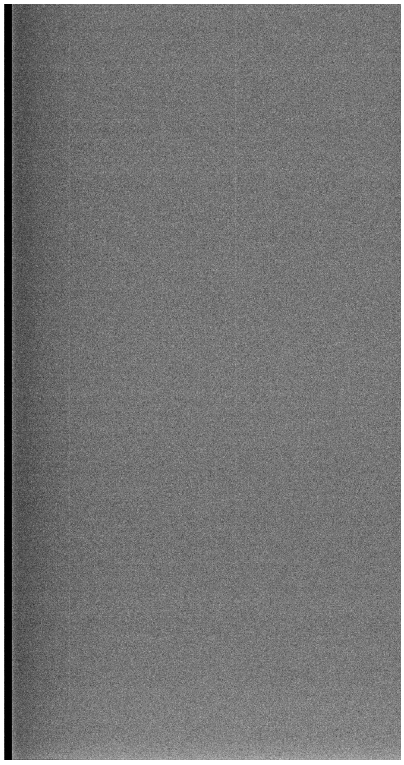


Cosmetic defects

The cosmetic quality of this chip is very good, showing only a couple of columns defect. The following images are the median stack of 5 bias and 5 long darks (1 hr). The dark image clearly shows the location of the 2 bad columns. The bias image only shows one column defect. The column defects are caused by hot pixels located at coordinates (1254,917) and (1973,3173).

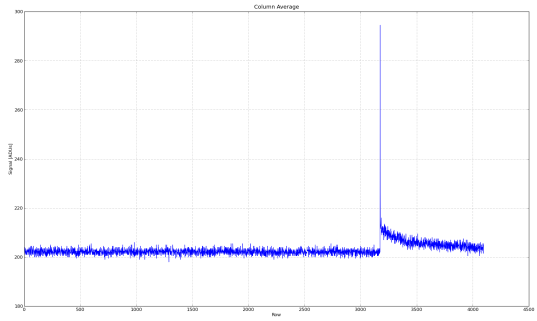


5 long dark median

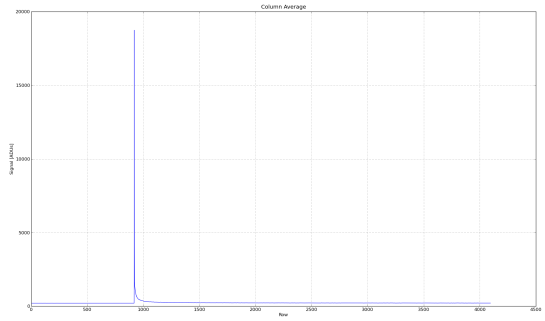


5 bias median

The following graphs shows traces of the columns affected by the hot pixels.

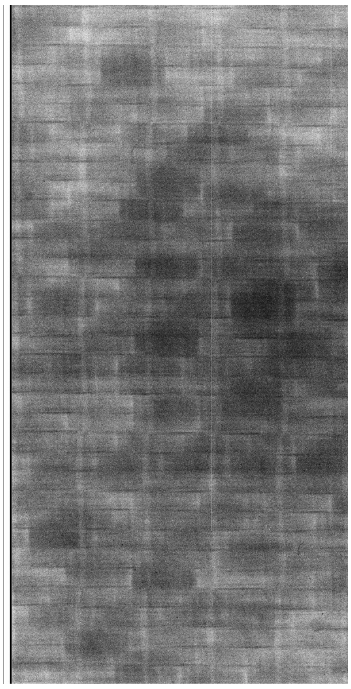


Hot Pixel @ 1253,917

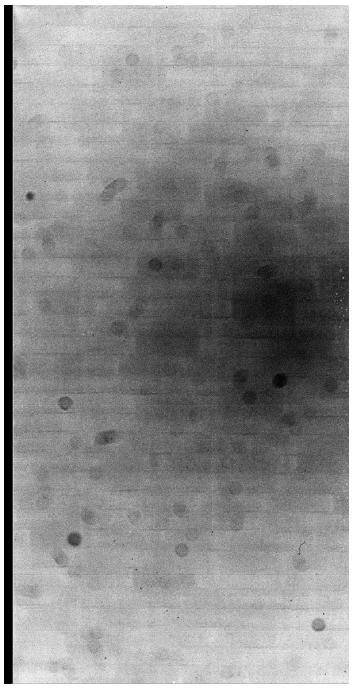


Hot Pixel @ 1973,3173

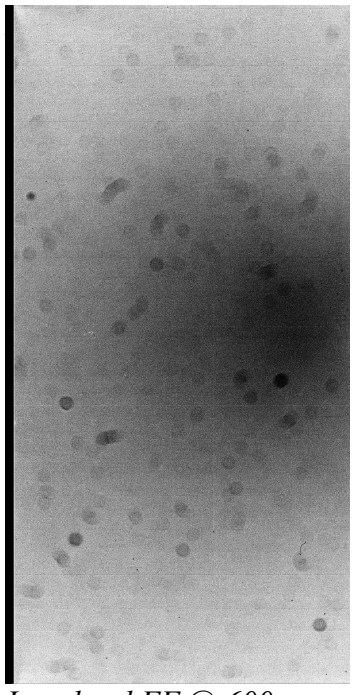
Images



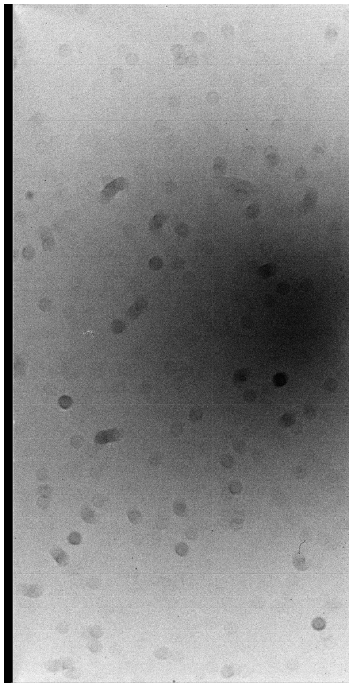
Low level FF @ 350nm



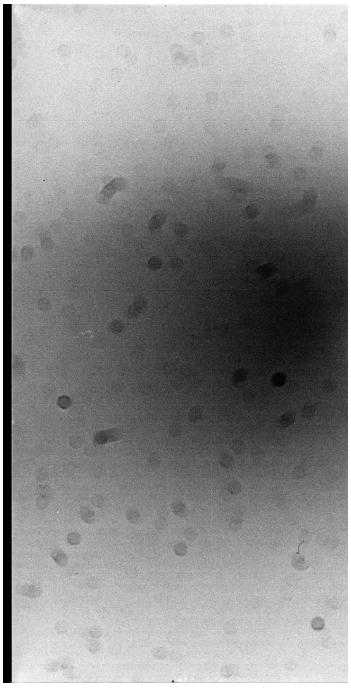
Low level FF @ 400nm



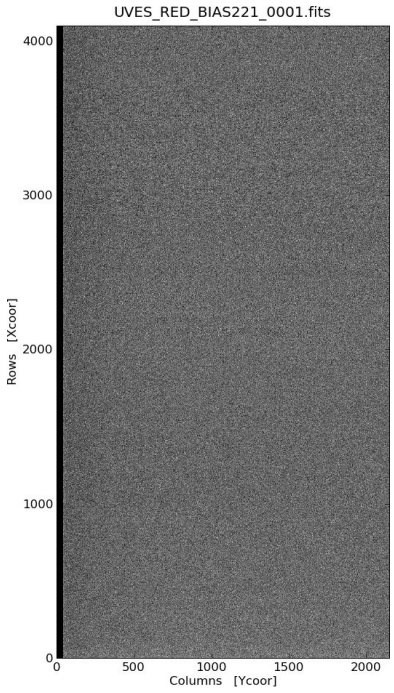
Low-level FF @ 600nm



Low level FF @ 750nm



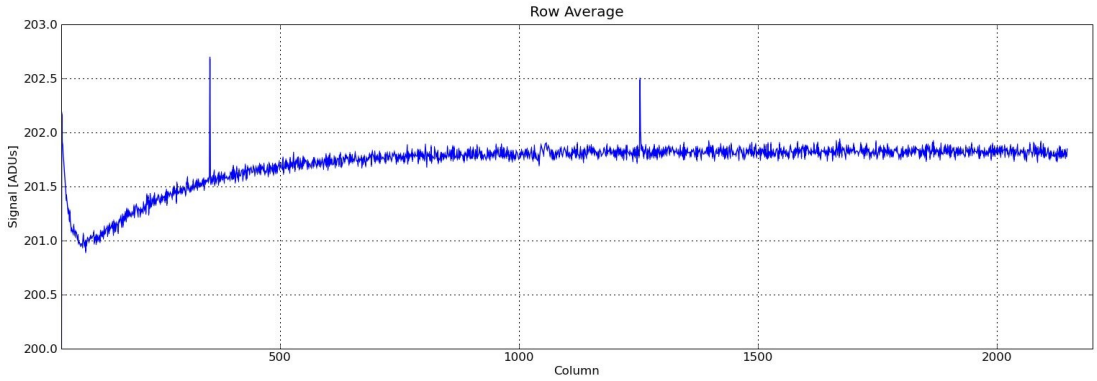
Low level FF @ 900nm

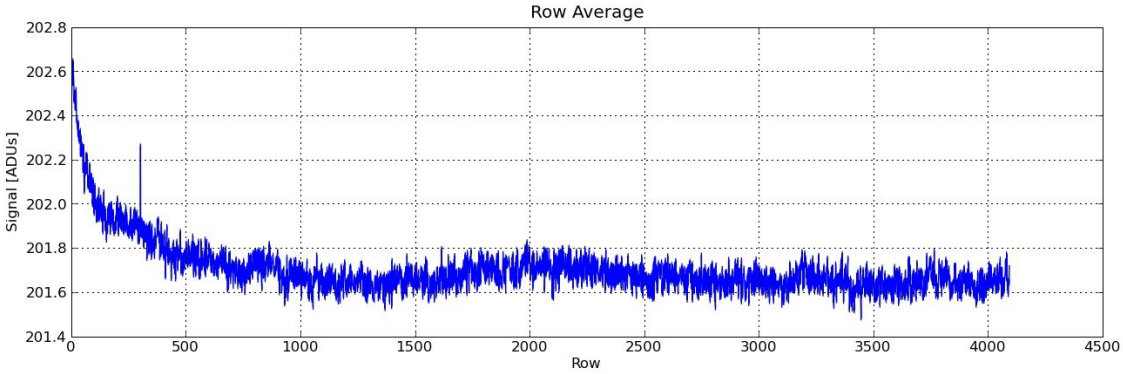


Bias Image

Bias and Dark spatial stability

The next graphs shows the plots of rows and columns collapsed for 5 bias images median stacked.

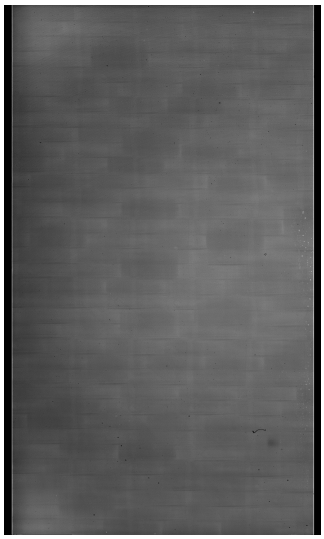




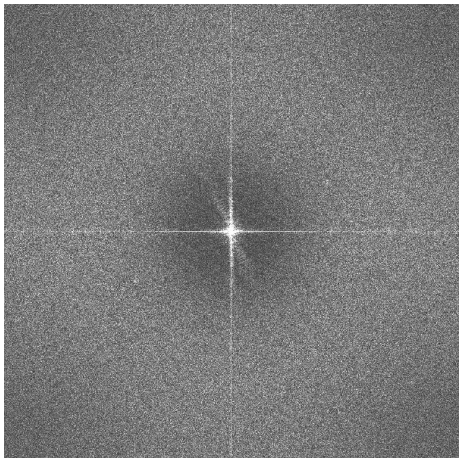
There is some ramping effect, but is less than 1 ADU peak to peak and stable.

Fixed Pattern Noise

Some testing was done in Paranal to check the fixed pattern noise. On the FF taken in Paranal the fixed pattern noise can be seen. A Fast Fourier Transform analysis clearly shows the FPN. Then we analyzed the FFT of the ratio between a high level FF and a low level flat field. This shows that the FPN is eliminated.

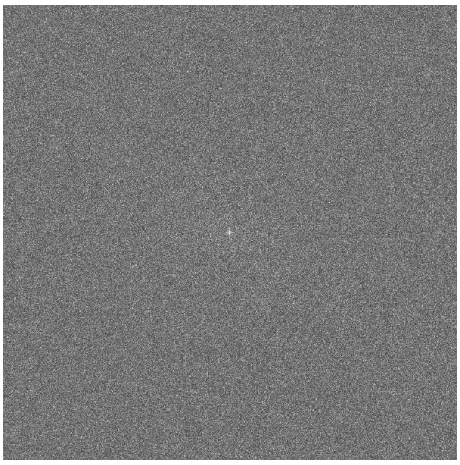


High level FF



2D FFT HL Flatfield

Ratio of 2 FF at different levels



2D FFT FF Ratio

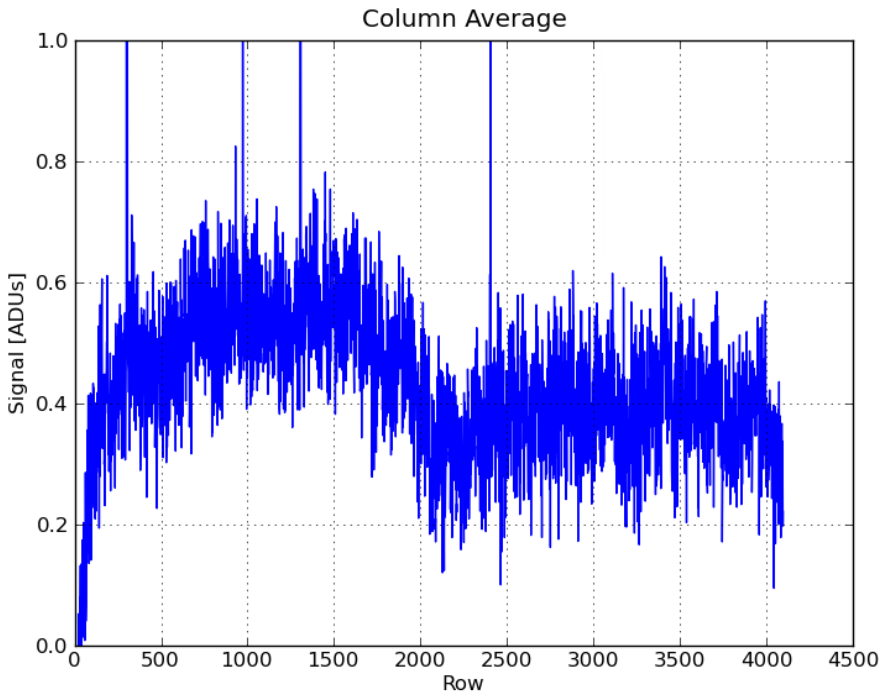
Dark Current

To compute the dark current, 5 bias exposures and 5 long dark of 1 hr were performed. This data set was used to compute the median image of the 5 bias and also of the darks. The executed median processing of the images eliminates the pixels affected by cosmic events.

Once we have the Master Bias and the Master Dark, using the above method, it is possible to subtract the Master Bias from the Master Dark to compute the dark current in ADUs generated in one hr.

The following graph shows the column average of the dark current image, as it can be seen, the dark current in ADUs is (in average) lower than 0.6 ADUs . To convert to electrons, the conversion factor for the 225kps/1x1/LG (1.5 e/ADU) is used.

In conclusion the dark current is lower than **0.9 e/pix/hr**



Cosmic ray hit

To determine the number of pixels affected by cosmic rays, 5 long dark (1 hr each) were taken. Then, for each dark image, the same sub area of 666 by 666 pixel (equivalent to 1 square cm) was selected and the median image for that area was computed. From the median image a threshold value was defined and all the pixels with an ADU level above the threshold were defined as cosmic ray affected.

Below are the sub image sections showing the Cosmic ray hits and a table with the number of pixel affected.

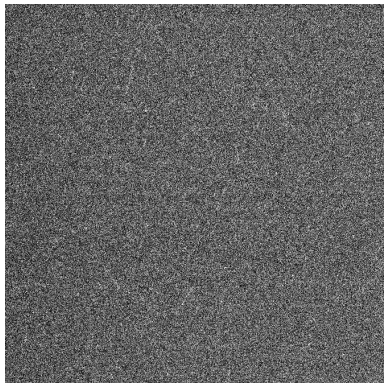


Illustration 1: Dark median

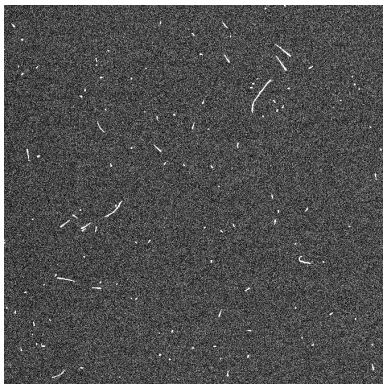


Illustration 2: Dark1

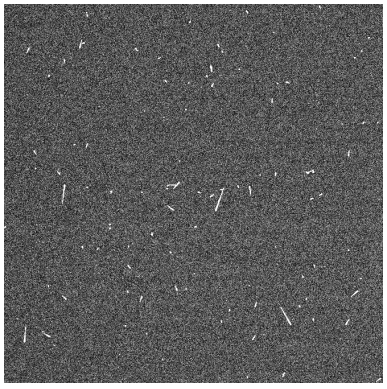


Illustration 3: Dark2

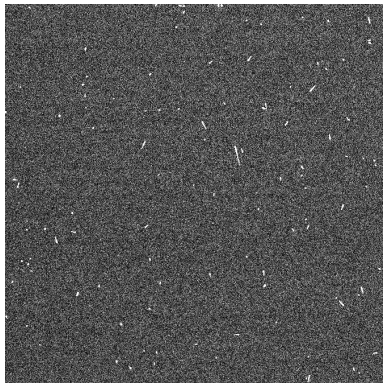


Illustration 4: Dark3

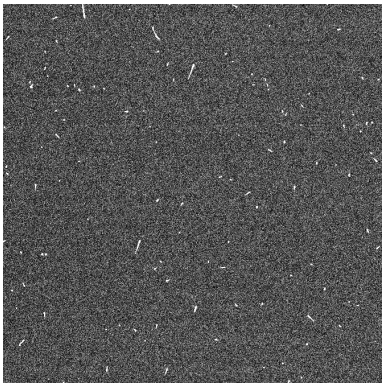


Illustration 5: Dark4

Illustration 6: Dark5

The table contains the number of pixels affected by cosmic events on each dark and the last two rows shows the average number of cosmic events per square cm per hr, and the percentage that it represent.

Image Name	**Number of Pixel hit by Cosmic Ray**
Dark1	1452
Dark2	1102
Dark3	942
Dark4	1041
Dark5	1185
Mean number of pixel affected	1144
% of pixel affected	**0.26%**

Vertical and Horizontal CTE

The inspection of long dark images and also the information provided by the manufacturer confirms that the CTE is very good both in vertical and horizontal direction. The values provided by the CCD manufacturer are:

VCTE=0.999999

HCTE=0.9999967

The CTE in the horizontal direction was measured using the Extended Pixel Edge Response (Scientific Charge-Coupled Devices, SPIE Press, James R. Janesick 2001). The UVES clock patterns include 50 over-scan pixels that were used to evaluate the HCTE. The value obtained by this method was:

HCTE= 0.999999

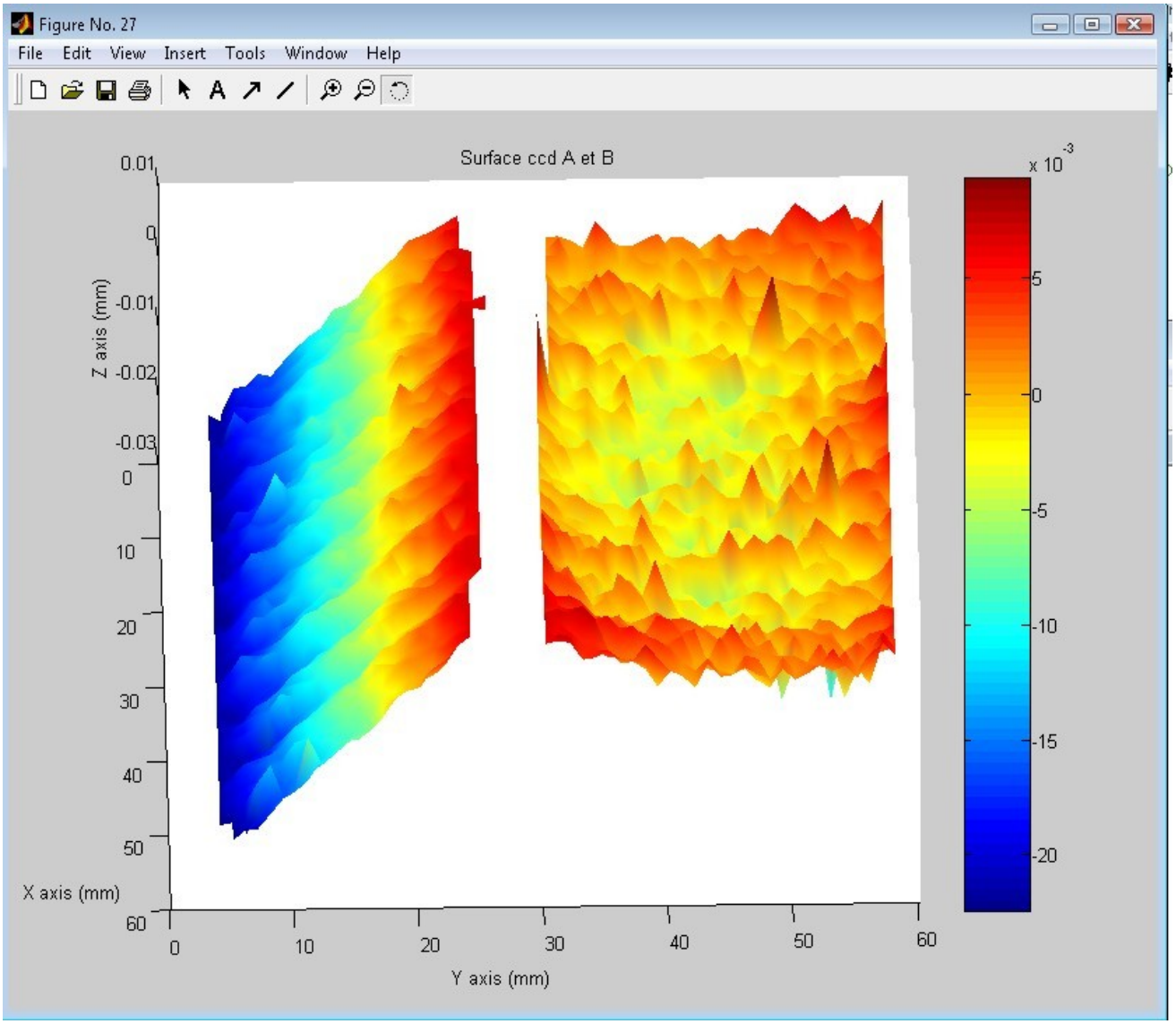
The clock patterns implemented for UVES don't include over-scan region in the vertical direction, so the value cited at the beginning of this document is the one provided by the CCD manufacturer but it's confirmed by the detailed analysis of the cosmic ray events.

CCD Alignment

For the MIT chip installation we used as a reference the EEV chip in the mosaic which was not touched during the MIT chip upgrade. After 2 iterations it was possible to achieve a peak to valley deviation of 29 +/- 5 um of the MIT chip surface with respect to the E2V chip surface. This was measured at 139K.

With respect to the gap between both chips, this was 1250 +- 50 mu at the bottom (close to the readout register), and 1470 +/50 um at the top.

The mounting assembly for the MIT chip did not allow any possibility to adjust this gap difference, but it has no impact in the data reduction and it has been compensated for in the data reduction pipe line.



MIT (left) and EEV surfaces after MIT alignment

Final installation in Paranal

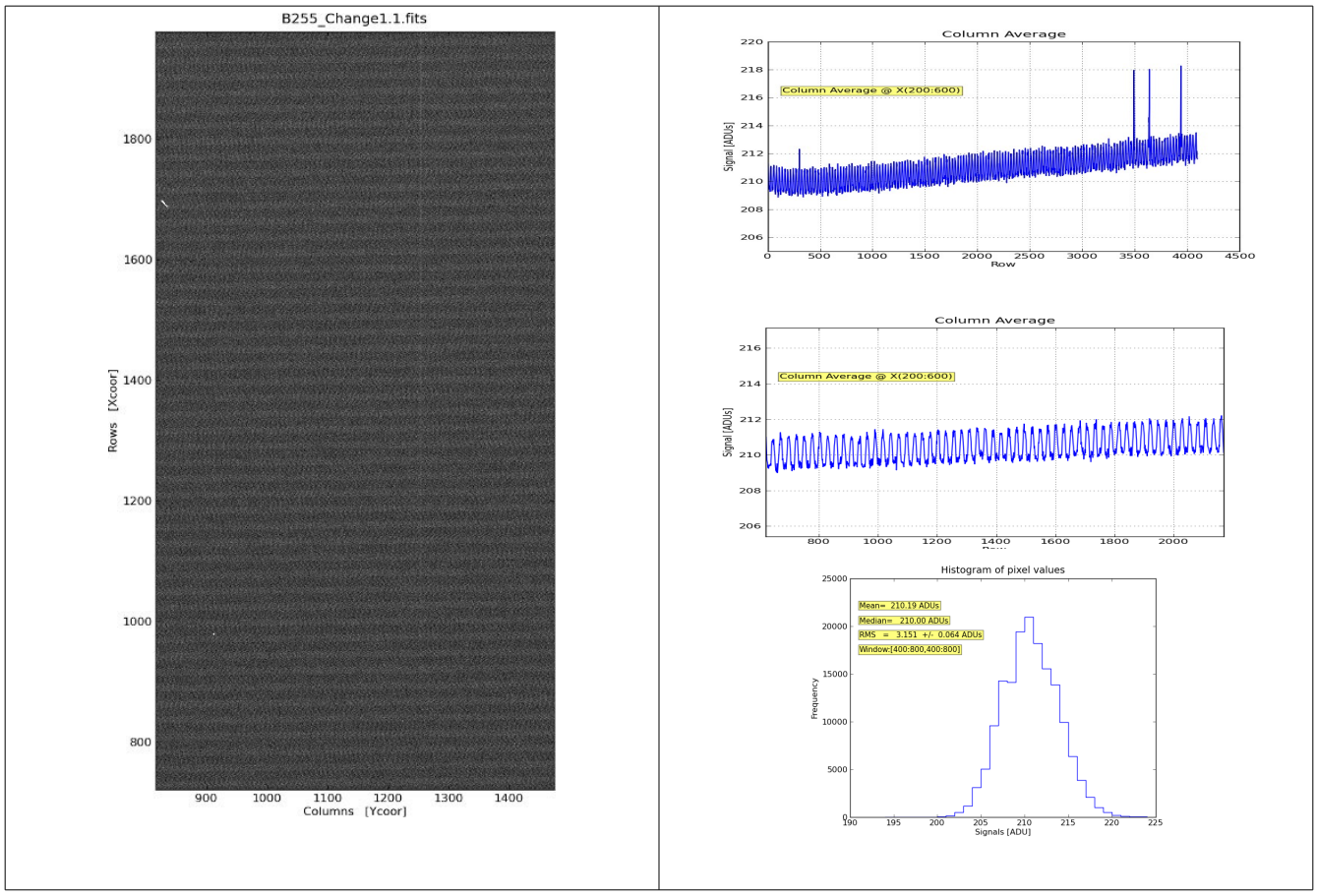
During the testing of the UVES RED cryostat in Paranal it was observed that some interference patterns were present in the images of the MIT chip and also the RON of the system was higher than with the Nigel CCD.

A thorough investigation was done trying to locate the interference source. It was discovered that the LN2 level sensor installed in the LN2 UVES RED tank was increasing the RON of the MIT chip but the pick up noise was still present.

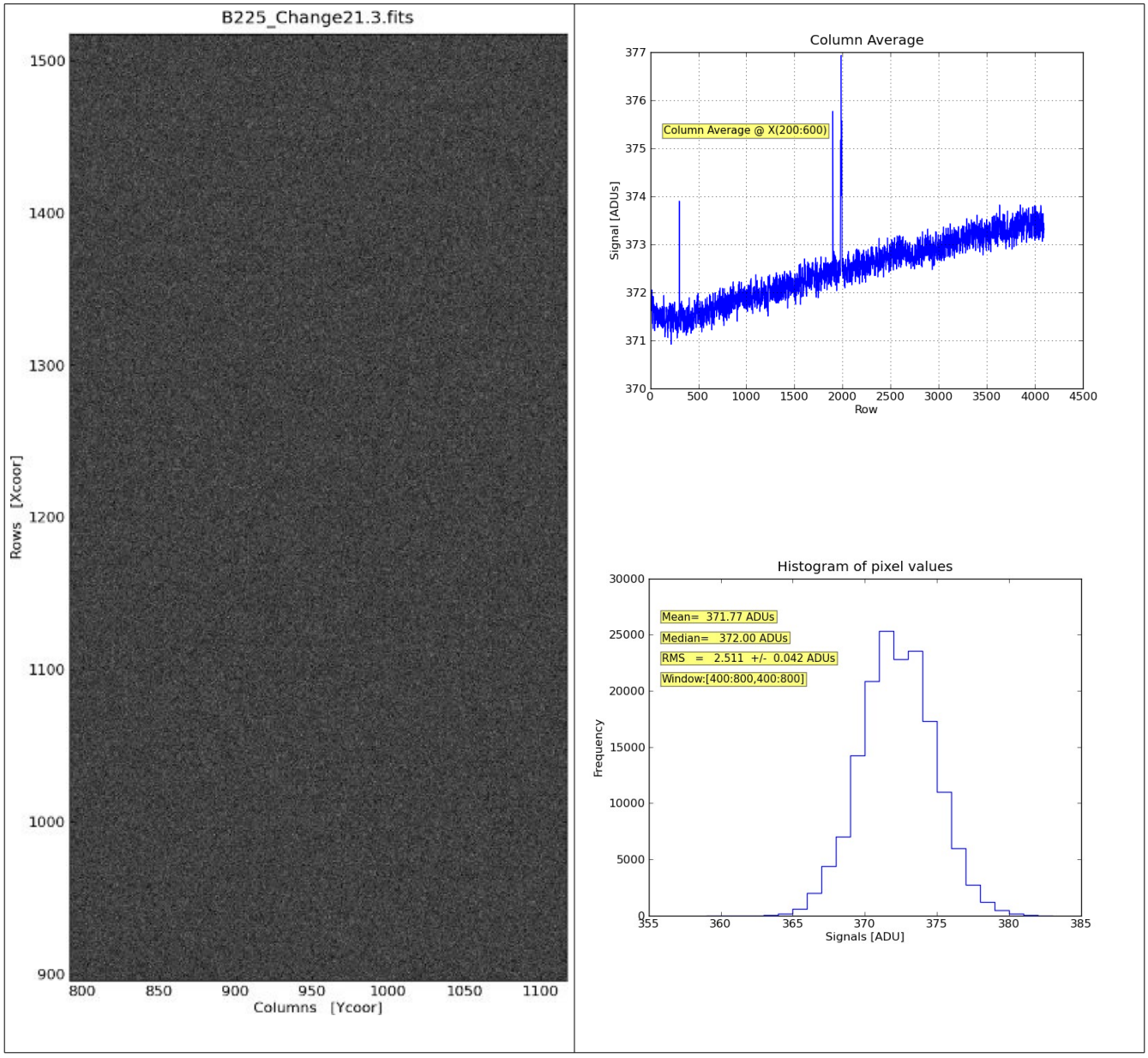
Different configurations of the DFE and PS FIERA boxes were tested and the best performance was achieved when the DFE electronic box was isolated from the rack where both the PS and the DFE are located.

To isolate the DFE from the metallic rack, it was enough to replace the 4 steel screws that hold the DFE box by 4 nylon ones.

The following images show the pick up pattern observed on the chip after installation in Paranal and without any change with respect to the grounding scheme used with the original MIT CCD (Nigel).

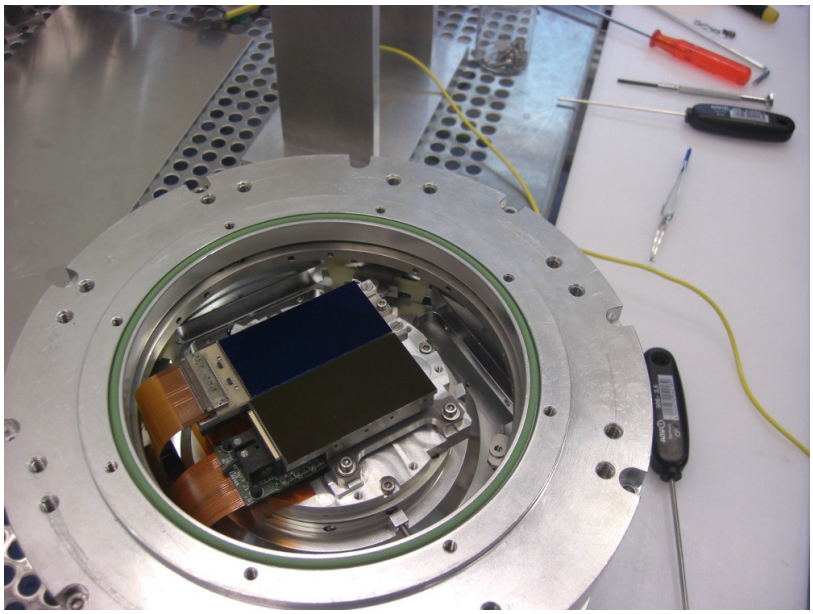


When both the LN2 level sensor was disconnected and the attachment of the DFE box to the aluminum frame was changed from steel screws to nylon screws, we got the following results:

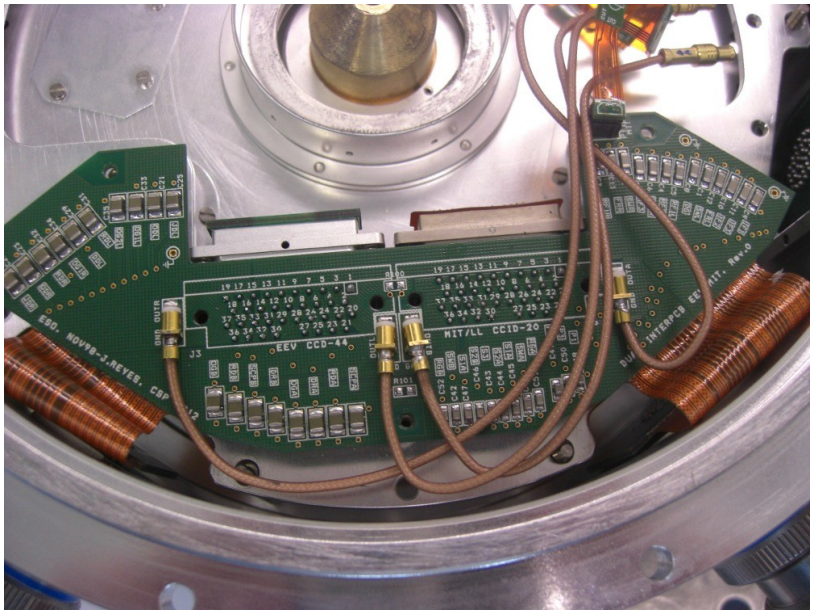


There is no pattern in the image, and the RON went from 3.15 ADUs down to 2.5 ADUs.

Photographs



The MIT chip (upper position) and the E2V chip in the detector head



InterPCB photo showing video outputs