Fundamental performance differences of CMOS and CCD imagers: Part IV

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ABSTRACT

This paper is a continuation of past papers written on fundamental performance differences of scientific CMOS and CCD imagers. New characterization results presented below include: 1). a new 1536 x 1536 x 8um 5TPPD pixel CMOS imager, 2). buried channel MOSFETs for random telegraph noise (RTN) and threshold reduction, 3) sub-electron noise pixels, 4) 'MIM pixel' for pixel sensitivity (V/e-) control, 5) '5TPPD RING pixel' for large pixel, high-speed charge transfer applications, 6) pixel-to-pixel blooming control, 7) buried channel photo gate pixels and CMOSCCDs, 8) substrate bias for deep depletion CMOS imagers, 9) CMOS dark spikes and dark current issues and 10) high energy radiation damage test data. Discussions are also given to a 1024 x 1024 x 16 um 5TPPD pixel imager currently in fabrication and new stitched CMOS imagers that are in the design phase including 4k x 4k x 10 um and 10k x 10k x 10 um imager formats.

Keywords: CMOS and CCD scientific imagers.

1. INTRODUCTION

Previous papers compared fundamental performance and operational differences for scientific CCD and CMOS imagers.[1-4] This important testing phase is nearing an end and is likely that most important characteristics have been uncovered (e.g., CMOS random telegraph noise (RTN) versus CCD flicker noise[2]). Future work and papers will now use findings by employing them into viable CMOS sensors for scientific imaging applications that require the highest performance possible (but not necessarily minimum cost as commercial CMOS must realize).

This paper reports specifically on test results for imagers fabricated on Sandbox V introduced in Ref. 1 (refer to Fig. 109). Sensors discussed are fabricated at Jazz Semiconductor, Newport Beach Ca., by employing their standard 3.3 V and 5.0 V - 0.18 um CMOS processes. Custom Sarnoff implants added to these processes to achieve high performance include 1) diode and pinning implants for the 5TPPD pixels, 2) a MOSFET buried channel to control RTN and threshold voltage, 3). a buried channel for photo gate (PG) and CMOSCCDs and 4) sense node contact to control dark current and leakage. Also, thick, high-resistivity epitaxial and SOI silicon wafers were custom manufactured for our imagers.

2. 1536 x 1536 5TPPD MINIMAL ARRAY

Figure 1 presents a 'first light' image generated by a new scientific 1536 x 1536 x 8 um 5T pinned photo diode (PPD) pixel CMOS imager introduced in Ref. 1 (referred to as the BIG MIN I array). Figure 2 shows the chip with 120 bond pads wired into a ceramic package. Figure 3 shows a packaged device installed into a low insertion force socket and camera head support electronics. The sensor can either be read through a single output port or by 16 ports for high-speed operation (as employed to generate Fig. 1). BIG MIN I was designed for global shutter (SNAP) readout using dCDS signal processing. The imager is currently being thinned for backside illumination.

Figure 4 presents a charge transfer efficiency (CTE) square-wave response taken from a row of BIG MIN I pixels demonstrating that deferred charge (image lag) is non existent with less than one electron measurement accuracy. Figure

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5 presents a photon transfer curve (PTC)[5] showing that the 5TPPD pixel achieves a charge capacity of 30,000 e- and an average read noise floor of 2.5 e- yielding a dynamic range of 12,000. A sense node sensitivity of 66 uV/e- is measured.

As illustrated in Fig. 6, the PPD potential (V_{PPD}) of the BIG MIN I pixel is set to approximately 1 V (via pinning and diode implant dose and energy). This level allows the sense node to swing up to 2 V assuming it is reset to V_{REF} = 3.5 V. The PPD potential of 1 V is generally applied to large (> 8um) 5TPPD pixels. In comparison for smaller pixel designs, the PPD limits charge capacity and requires a higher potential (typically V_{PPD} =1.5 V for 3.3 V operation). In addition to greater dynamic range, CTE performance is enhanced with a lower PPD potential because fringing electric fields between the PPD and sense node regions are stronger to assist small signal transfer. Higher fields reduce surface state trapping and curtail barrier problems related to the transfer gate (TG) if such problems exist.[1]

Ideally, the positive TG clock drive required to transfer charge should be approximately equal to the V_{PPD}. However, additional TG clock swing beyond V_{PPD} is usually necessary to achieve perfect charge transfer as V_{PPD} increases. For example, Fig. 7 plots the CTE break point voltage (V_{CTE}) as a function of V_{PPD} for a group of ten silicon wafers with different PPD implants. Note that V_{CTE} grows faster than V_{PPD}. This is undesirable characteristic limits the amount of TG drive that can be utilized (e.g., TG potential must be less than sense node voltage or read noise will increase slightly[1]).

PPD potential data shown in Fig. 7 is generated by two different measuring techniques. The first method is based on Fig. 8 that plots the output response of a 3TPPD pixel as it integrates signal charge after being reset. Both the sense node and source follower output responses are shown. In that the 3TPPD pixel is fabricated identically to the 5TPPD pixel it can be used to determine V_{PPD}. As can be seen, the sense node response is linear with time up to a potential of approximately 2.1 V. Beyond 2.1 V the response is non linear which indicates the PPD has left depletion. Hence, charge coupling and full depletion for the 5TPPD pixel occurs when V_{PPD} = 2.1 V.

The second test method to determine V_{PPD} and cross check the first method uses the 5TPPD pixel directly (refer to Fig. 9). First, the low level of the TG clock (TG_{LOW}) is increased as indicated by the arrow. At some value of TG_{LOW} signal charge contained in the PPD region will begin to 'bloom' onto the sense node. For example, the lower raw video trace of Fig 10 shows such blooming taking place (i.e., $TG_{LOW} > V_{PPD}$). The onset of blooming is when $V_{PPD} = TG_{LOW}$ which for the sensor is 2.1 V agreeing with 3TPPD measurements above. Note it is important for this measurement to use a very low signal level to not disturb the PPD potential or blooming will take place prematurely producing a V_{PPD} value lower than it really is.

3. ADVANCED AND FUTURE DESIGNS

BIG MIN I is followed by a 1024 x 1024 x 16 um 5TPPD imager currently in fabrication on Sandbox VI (refer to Fig. 110). Called the BIG MIN II imager, Fig. 11 presents a block format diagram of the imager showing four 512 x 512 pixel quadrants each having; 1) X-Y address decoder, 2) pixel clock drivers, 3) column aCDS/dCDS analog signal processors, 4) column multiplexer and 5) output source follower buffer. There are many different ways to read the imager. For example, if desired each quadrant can be addressed and read out independently from its neighbors.

Figure 12 shows the sub-electron noise signal chain contained in each column of the BIG MIN II imager (for a total of 2048 circuits). Signal from the pixel can be amplified by a low noise pre-amp which offers different gain settings (2, 3, 4, 8 V/V) or the circuitry can be completely circumvented for unity gain operation by externally commanding the 2:1 transmission switch shown. A second 1:2 transmission switch can take pixel video directly to an output buffer (dCDS signal processing uses this channel). The same switch can also direct video into the aCDS processor which includes a clamp and dual sample and hold circuitry. The dual sampler eliminates row settling time by allowing the user to process a row of pixels while a subsequent row is encoded by an off-chip ADC (single sampling can be employed if desired). The aCDS circuits are designed to support a 2 V output pixel signal swing and the MUX can be scanned up to 50 MHz for fast encoding purposes by an off-chip ADC (ideally by 14 and 16 bit ADCs).

The large storage capacitors used in the clamp and sample circuits are selected such that kTC switching noise is below one electron. Figure 13 plots kTC noise (rms e-) as a function of capacitance and capacitance area for various sense node gains (V/e-). The storage capacitors must be >2 pF assuming 50 uV/e- to achieve sub-electron noise performance.

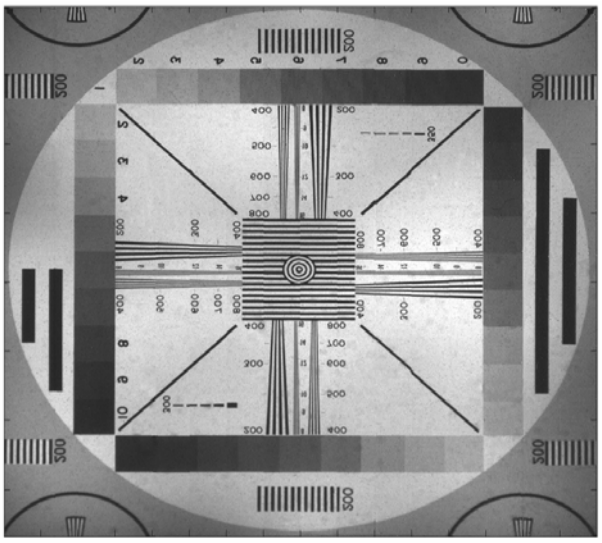

Figure 1. 5TPPD 1536 x 1536 BIG MIN I test pattern image.

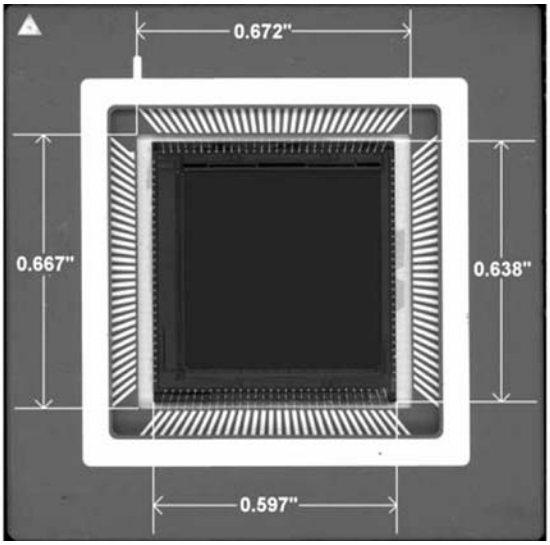

Figure 2. Packaged BIG MIN I imager.

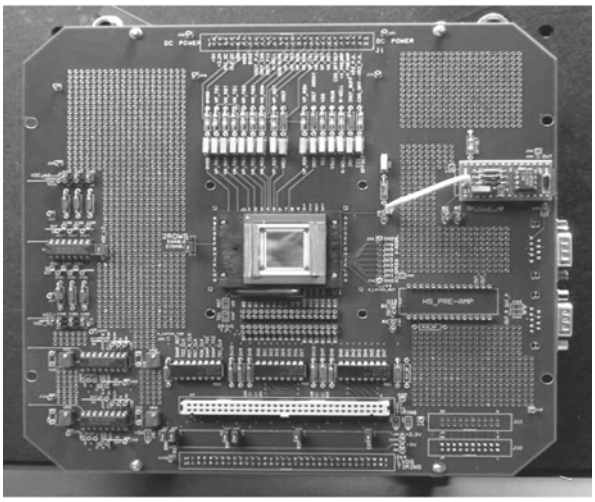

Figure 3. BIG MIN I evaluation test board.

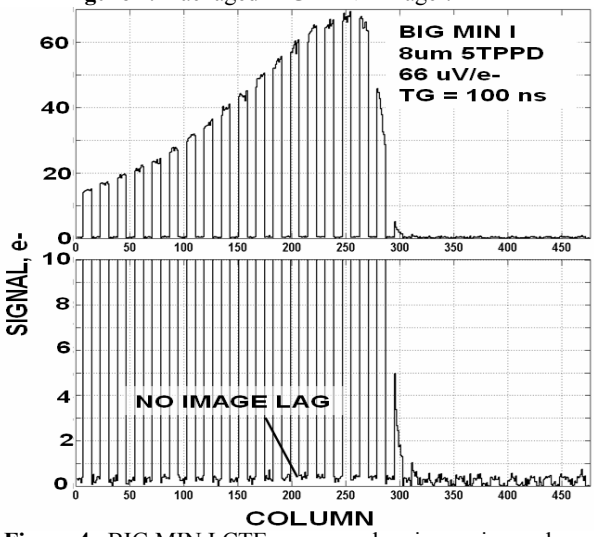

Figure 4. BIG MIN I CTE response showing no image lag.

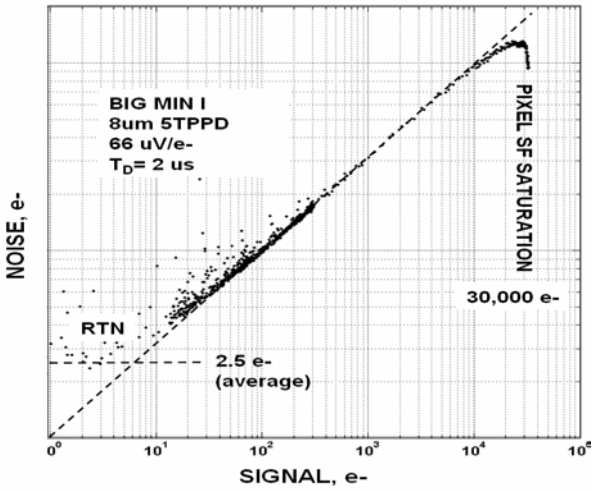

Figure 5. BIG MIN I photon transfer curve (PTC).

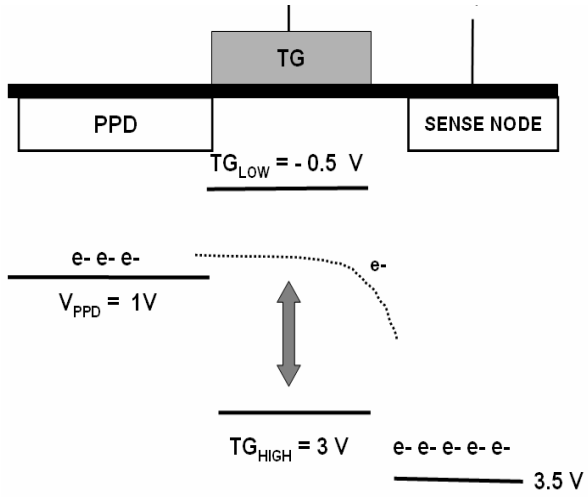

Figure 6. PPD pixel process set up potentials.

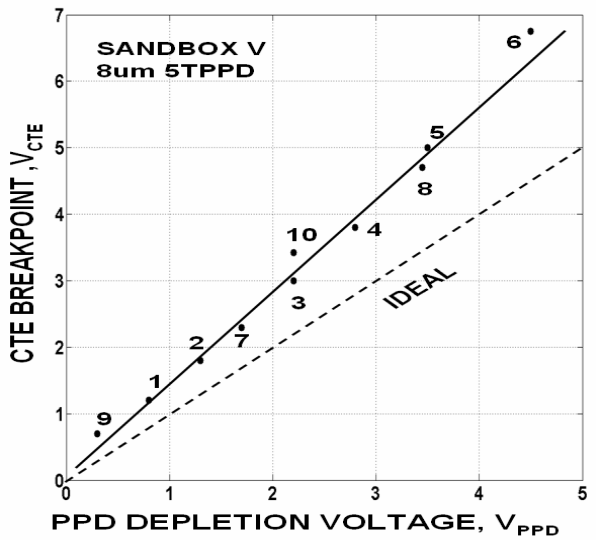

Figure 7. CTE breakpoint with depletion voltage.

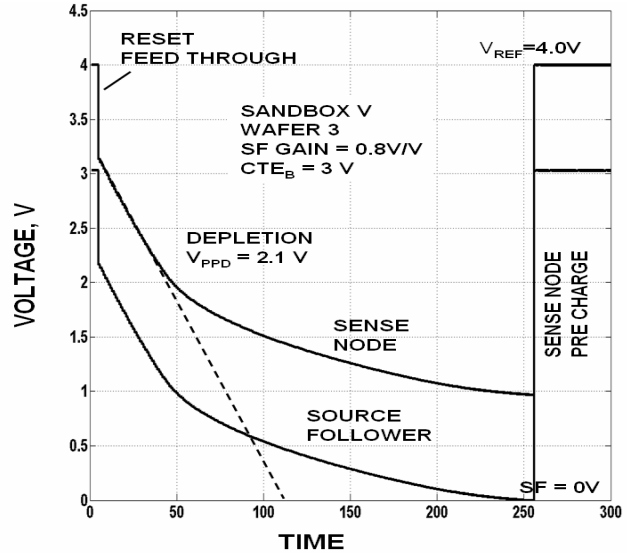

Figure 8. 3TPPD method to measure 5TPPD depletion voltage.

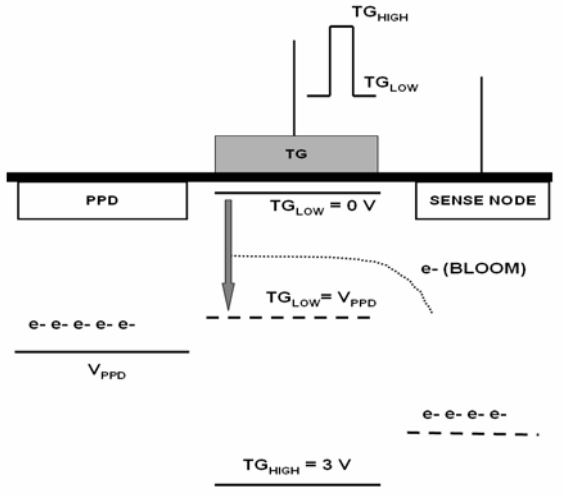

Figure 9. 5TPPD pixel technique to measure depletion voltage.

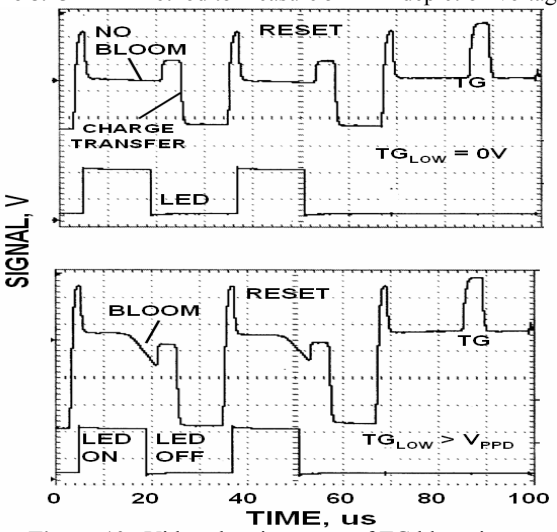

Figure 10. Video showing onset of TG blooming.

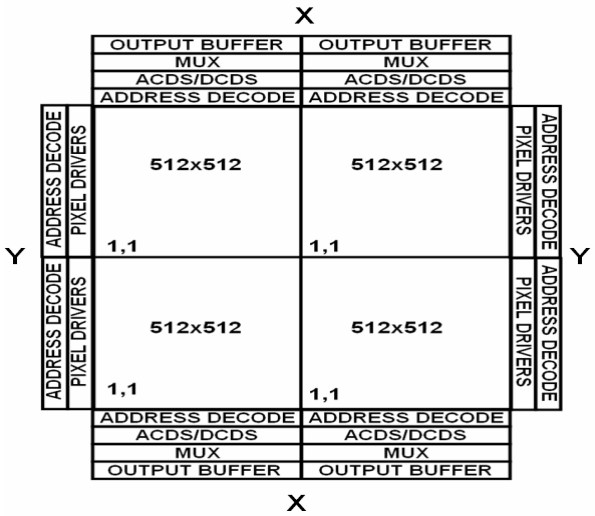

Figure 11. Big Min II imager layout.

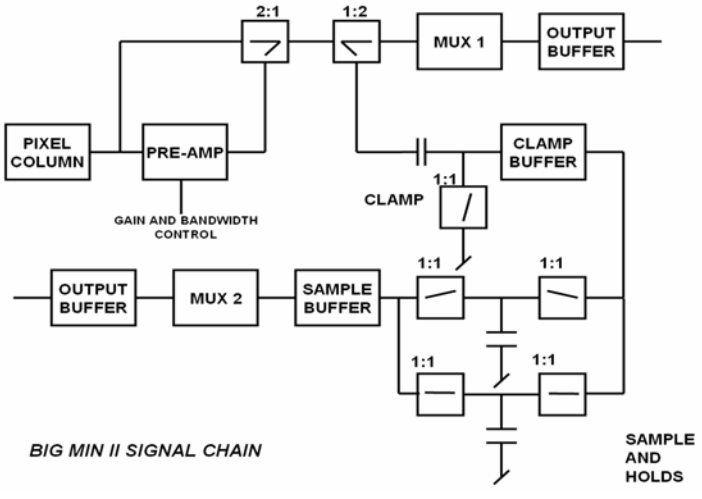

Figure 12. Big Min II sub electron signal chain.

However, additional capacitance is required for pixel arrays with less V/e- sensitivity. Six pico-farad capacitors were selected for BIG MIN II for the variety of future pixels anticipated that will use the circuitry. Figure 14 shows a Fe-55 x-ray response generated by a 256 x 256 x 16 um 5TPPD imager with an on-chip column clamp switch that uses a 6pF capacitor. The measurement shows that only pixel source follower noise is present and that kTC noise related to the clamp capacitor is negligible (i.e., sub-electron).

The design of BIG MIN II is configured for 'stitched' formats for large chip sizes.[1] Figure 15 shows a block diagram illustrating how a new 4k x 4 k x 10 um 5TPPD imager is planning to be 'stitched' following similar layout features as BIG MIN II. Note that the sensor is configured into sixteen individual 1k x 1k blocks surrounded by 'enable' lines used to control various readout modes and minimize the number of address lines and bond pads. For example, to simultaneously read the lower four 1k x 1k blocks control enable lines $E_X(1,B)$ / $E_X(2,B)$ / $E_X(3,B)$ / $E_X(4,B)$ and $E_Y(L,1)$ / $E_Y(R,1)$ are selected. In turn the X-Y addresses, pixel drivers, aCDS signal chains and the four output buffers are activated for readout. On the other hand, if only the lower left hand corner segment is required, $E_X(1,B)$ and $E_y(L,1)$ lines are activated. Non activated blocks consume considerably less power. The format structure can also be extended to 6k x 6k, 8k x 8k and 10k x 10k imagers as shown in Fig. 16. Currently 4k x 4k and 10k x 10k imagers are in the design phase for Sandbox VIII.

4. BURIED CHANNEL MOSFETS

Advantages for operating the pixel's source follower buried channel are to reduce random telegraph noise (RTN) and MOSFET threshold voltage for greater signal dynamic range.[1] Figure 17 compares noise performance for an 8 um 3TPPD Minimal Array which incorporates both buried and surface channel source follower amplifiers. The top 3D noise plot shows significantly less RTN for the buried channel pixels. The noise test assumes an aCDS bandwidth of 125 kHz (equivalent to a signal chain dominant time constant of T_D = 2 us) and produces 'average' read noise levels of 1.97 and 3.3 e- for the buried and surface channel MOSFETs respectively. Figure 18 reduces the bandwidth to 42 kHz (T_D = 6 us) which in turn lowers noise floor to 0.96 e- and 1.89 e-. Figure 19 presents noise histograms for Figs. 17 and 18 using a log-linear scale. The 'RTN skirt' width seen is considerably less for the buried channel operation.

Figure 20 shows RTN dark images for a single row of surface channel pixels that are read as a function of time assuming T_D = 6 us and T_D = 2 us. Some RTN decreases with bandwidth reduction. Figure 21 quantifies the noise for two rows of pixels with and without buried channel source followers. The buried channel row generates average noise levels of 2.12 e- and 1.03 e- for the two bandwidth settings (T_D=2 us and 6 us) whereas surface channel produces noise levels of 3.6 e- and 2.02 e-. Note that the noise reduction with bandwidth is primarily associated with a decrease in white and background 1/f noise with only some RTN reduction taking place. This observation is seen more clearly in Fig. 22 where a row of surface channel pixels for the two bandwidth settings are differenced to produce the bottom trace. Note that only a few RTN pixels show a significant drop in noise level. These specific pixels exhibit a higher switching frequency compared to other RTN pixels, and therefore, are more responsive to the bandwidth change.

Figure 23 shows noise stacking plots generated by four Minimal Arrays with different buried channel implants. Surface channel devices are also in the plots to monitor noise improvement. The source follower MOSFET thresholds are labeled and can be compared to the standard surface channel threshold of V_T = 1.2 V. For example, Wafer 1 exhibits V_T= 0.85 V which is 0.35 V lower than its surface channel counterpart. As can be seen, RTN for Wafer 1 is approximately 1/2 of the surface channel device indicating less than optimum. Wafers 2 and 3 exhibit lower thresholds and produce lower RTN. Wafer 6 provides a deeper buried channel and achieves the lowest RTN floor (the imager tested in Fig. 17 and 18 comes from this wafer).

Also integrated into the plots of Fig. 23 are source followers with two different channel widths (minimum and 4x minimum). In general, wider channels generate less RTN at the expense of lowering V/e-.[1] Figures 24 and 25 present noise histograms for buried and surface channel amplifiers for channel widths A and B keeping the gate length fixed. Note that the RTN for the buried channel source follower with width B is nearly absent.

In addition to lowering RTN noise, the buried channel implant reduces the MOSFET threshold.[1] This feature is advantageous because the dynamic range of the source follower can be increased with greater output swing. For example, Fig. 26 plots source voltage as a function of gate voltage (V_{REF}) for surface and buried channel source follower

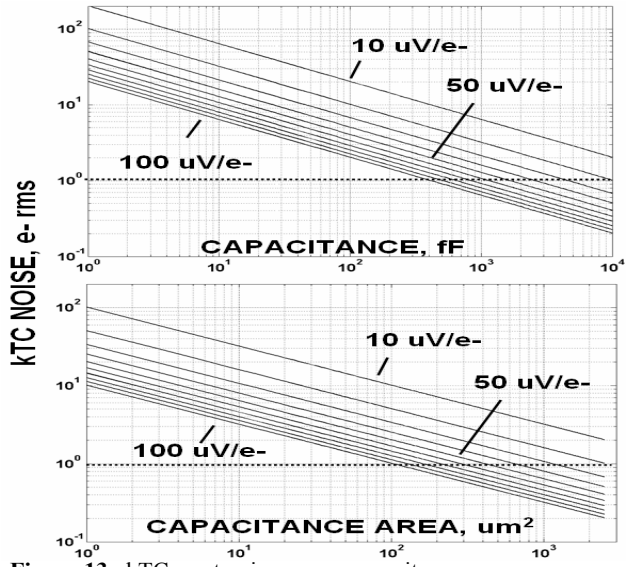

Figure 13. kTC reset noise versus capacitance.

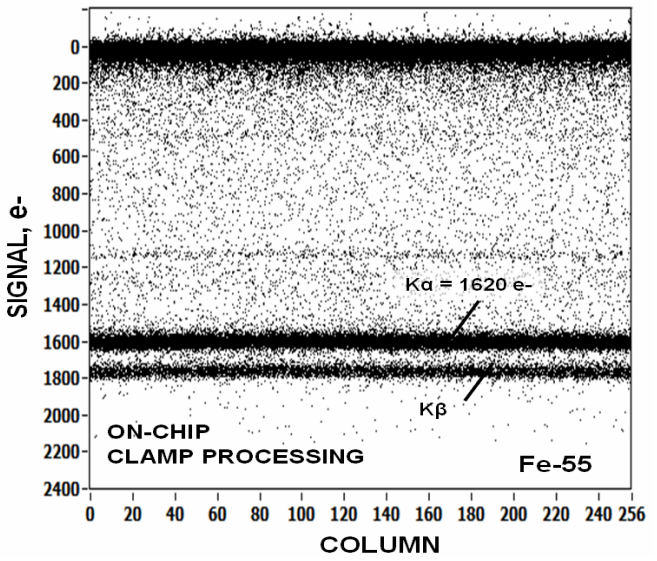

Figure 14. 5TPPD Fe-55 x-ray response of on-chip signal chain.

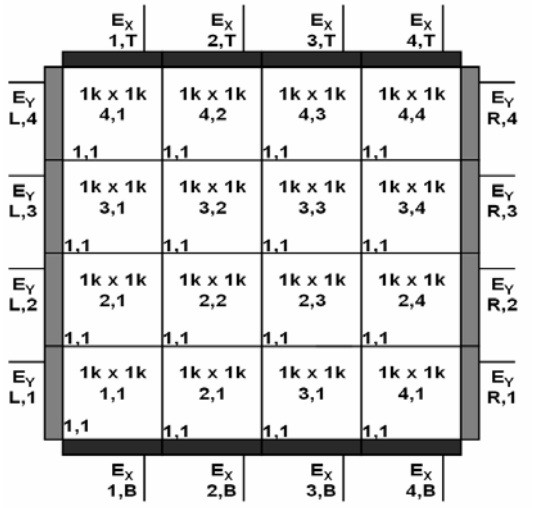

Figure 15. Block diagram of a stitched 4k x 4k imager.

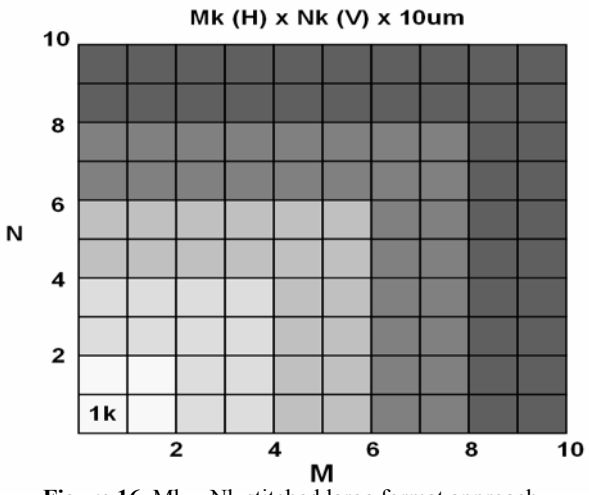

Figure 16. Mk x Nk stitched large format approach.

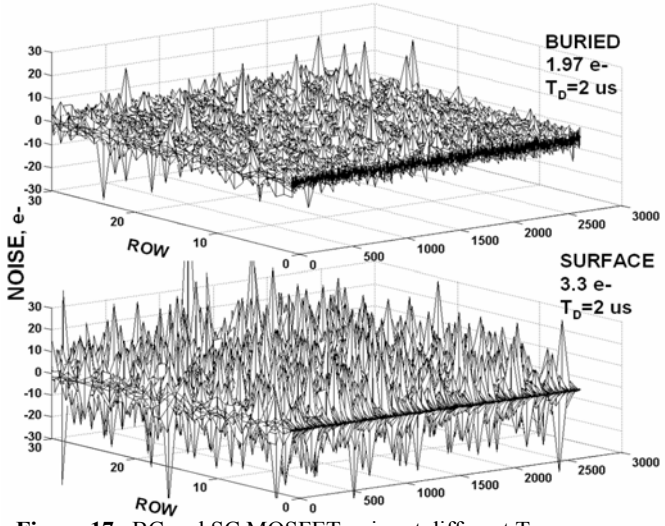

Figure 17. BC and SC MOSFET noise at different T_D.

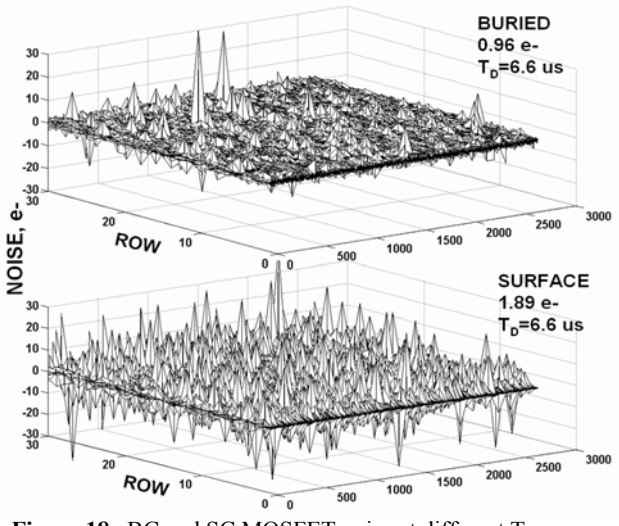

Figure 18. BC and SC MOSFET noise at different T_D.

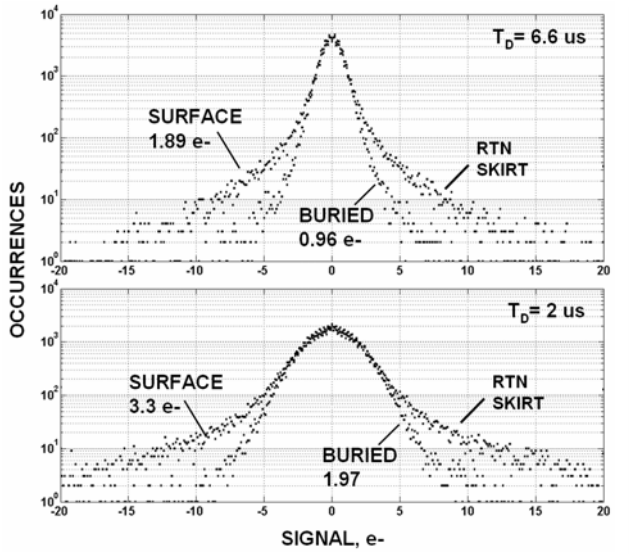

Figure 19. BC and SC noise histograms at different T_D.

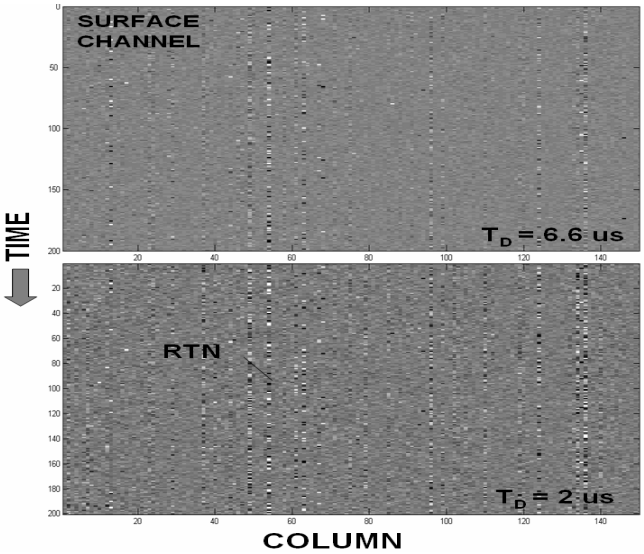

Figure 20. SC RTN dark images at different T_D.

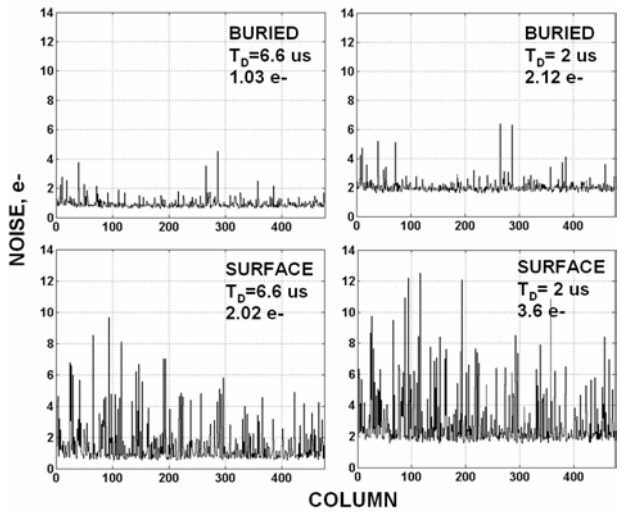

Figure 21. SC and BC RTN characteristics at different T_D.

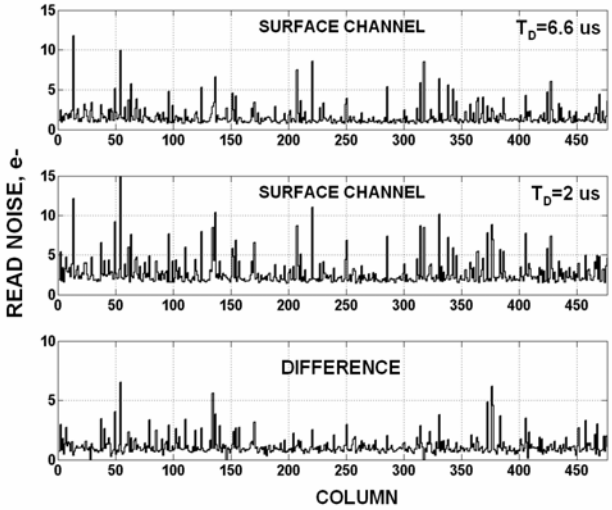

Figure 22. SC RTN characteristics at different T_D.

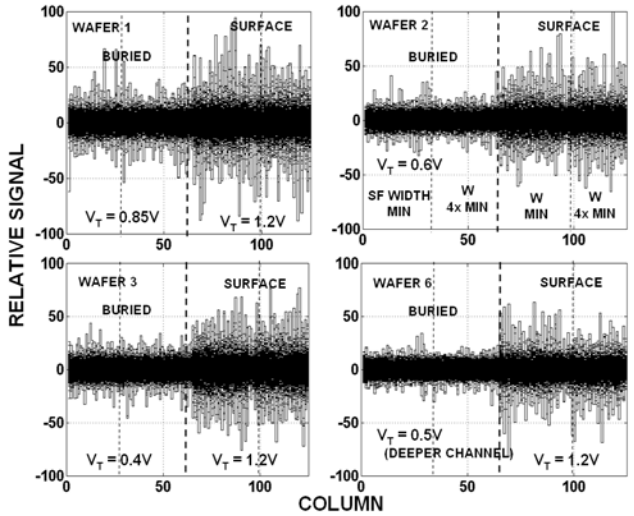

Figure 23. BC and SC noise plots with different buried channel implants.

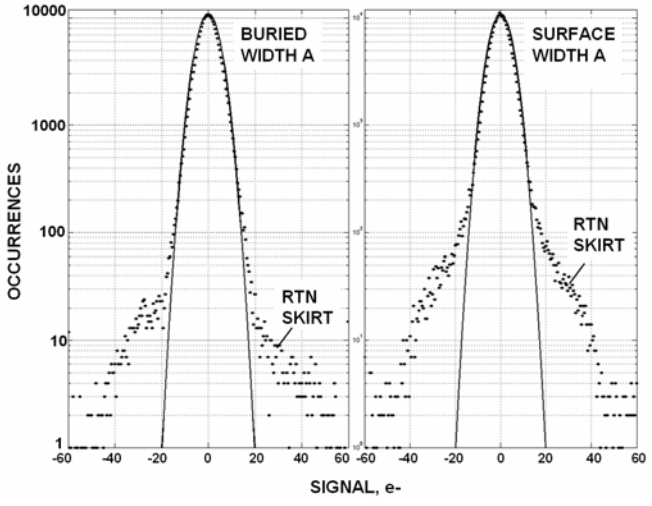

Figure 24. BC and SC noise histograms.

MOSFETs used on a 5TPPD pixel. For the nominal bias indicated (V_{REF} = 3.3V) and zero signal on the sense node, the buried channel source voltage is 2.75 V compared to 2.05 V for surface channel. The difference provides the source follower 0.7 V more head room to operate. The buried channel implant is also applied to the reset MOSFET channel. In doing so, the reset clock level can be lowered to achieve the 'hard reset' condition. This in turn increases dynamic range by reducing reset clock feedthrough. Figure 27 plots the reset clock level as a function of V_{REF} to obtain hard reset for buried and surface channel MOSFETs for a 3TPPD pixel. Note that the threshold is nearly eliminated for buried channel MOSFET requiring only a reset clock level of slightly more than V_{REF} whereas the surface channel requires >1 V more drive.

5. SUB-ELECTRON PIXELS

Figure 28 presents PTCs generated by a single buried channel 3TPPD pixel selected from Fig. 17 without apparent RTN. The PTCs are displayed in both DN and electron units. Data was generated by first resetting the pixel, then clamping the reset level to ground (to remove reset noise), followed by releasing the clamp at which time a pulsed LED is turned on for a fixed time period. Next the LED is turned off and the resultant video sampled thus completing the aCDS processing cycle. This sequence is repeated at various LED light levels to produce the PTCs shown. Note that a 0.78 e- noise floor is achieved for a dominant time constant of T_D = 6 us. This data demonstrates that 'sub- electron' noise is possible for CMOS imagers and could be realized for all pixels if RTN was not present. This of course is the end goal for using buried channel MOSFETs. Figure 29 shows a 20 e- square-wave image generated by turning the LED 'on and off' for the same pixel. Part way into readout the voltage to the LED is slowly lowered to reduce the signal level into the read noise floor. Figure 30 'stacks' column traces of the image showing the 4.5 e- photon shot noise and 0.78 e- read noise floors.

Proper aCDS/dCDS signal processing to achieve sub-electron noise performance as demonstrated above can be tricky. For example, a single noise electron from reset remnant noise[6] becomes problematic to the ideal read noise floor. For example, Fig. 31 plots reset remnant noise for a 3TPPD pixel as a function of reset-to-clamp release time assuming T_D = 4 us. Note that remnant noise slowly decreases until the true source follower noise floor of 1 e- is reached, but only after settling $5T_D$ time constants. Beyond 40 us the noise decreases further because the clamp-to-sample time becomes too short to maintain V/V gain. For maximum S/N, optimum processing time is when reset to clamp and clamp-to-sample time are equal which for this plot occurs at 31 us.

6. MIM PIXEL

Figure 32 illustrates the design of the "MIM pixel' introduced in Ref. 1. Note that the custom pixel includes an additional MOSFET (called the MIM MOSFET) and a 'metal –insulator –metal (MIM) capacitor that controls sense node sensitivity (V/e-). The MIM MOSFET can be incorporated into either 3T, 5T CMOS pixels or CMOSCCDs. The switch is usually globally activated by a single on-chip driver to switch the MIM capacitor onto the sense node. Figure 33 shows data generated by a single 24 um 3TPPD MIM test pixel being switched between the two gain states as the LED light source is switched on and off.

Figure 34 shows a different MIM pixel in response to Fe-55 x-rays where the sensitivity switches from 31 to 3.7 uV/e-. Figure 35 magnifies this plot showing good separation of the K-α and K-β lines indicating that low noise performance is maintained for low gain state. Figure 36 and 37 show PTCs that exercise the two gain states (expressed in DN and electron units). Note that electron read noise approximately scales with the gain change (i.e., 2.4 e-/DN and 0.38 e-/DN) whereas DN noise levels are nearly equal for both gain states. This is because read noise is generated by the pixel's source follower down stream of the sense node.

The addition of a n+ source diffusion required by the MIM MOSFET shown in Fig. 32 increases the sense node capacitance by approximately 1 fF. This in turn lowers the sensitivity for the high gain state and increases read noise compared to a pixel without the MIM switch. This problem can be circumvented by using the arrangement shown in Fig. 38 where the MIM MOSFET and reset MOSFET are placed in 'series' and clocked together to reset the sense node (such MIM pixel types are on Sandbox VI). Following the reset, the MIM switch is either turned off (for high V/e-) or left on (for low V/e-). Figure 39 plots V/e- as a function of MIM capacitance comparing the series and parallel arrangements assuming n+ diffusion and source follower gate capacitances of 1 and 1.5 fF respectively. Note the extra

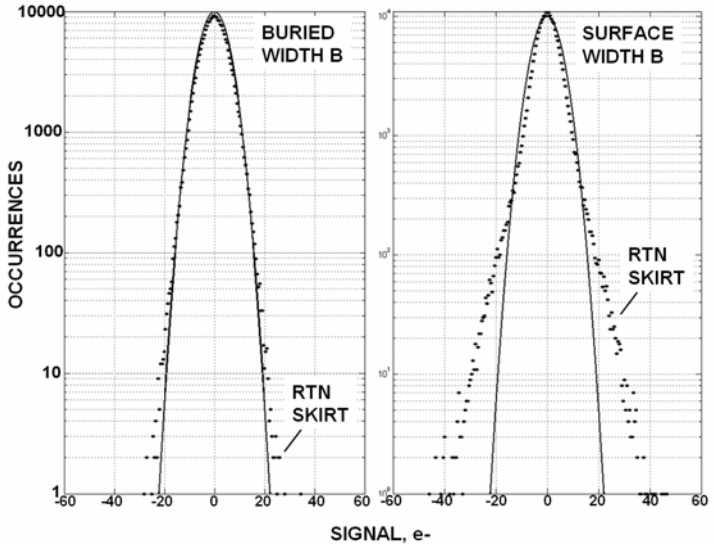

Figure 25. BC and SC noise histograms with wider channel.

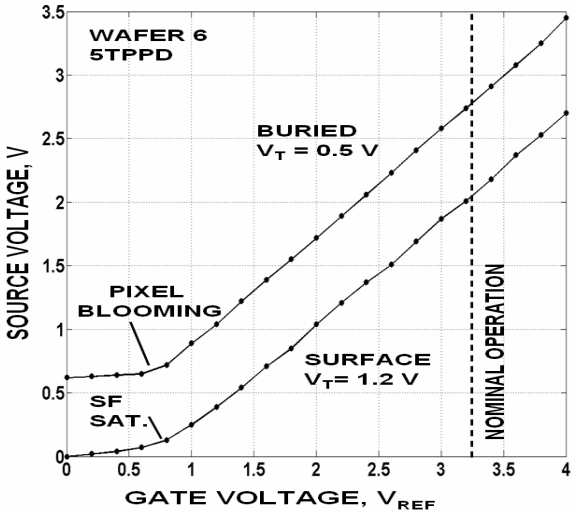

Figure 26. BC and SC threshold plots for SF MOSFET.

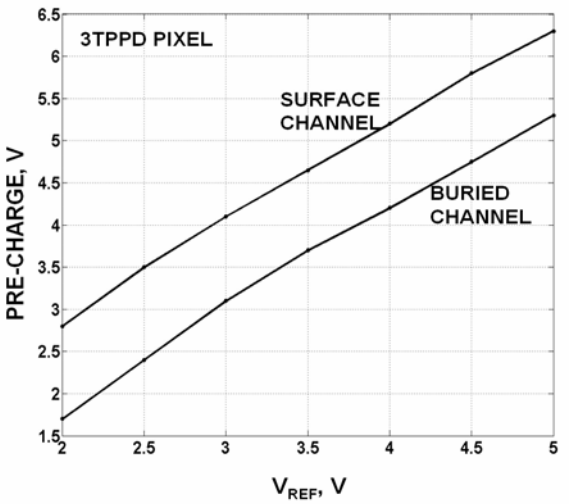

Figure 27. BC and SC threshold plots for reset MOSFET.

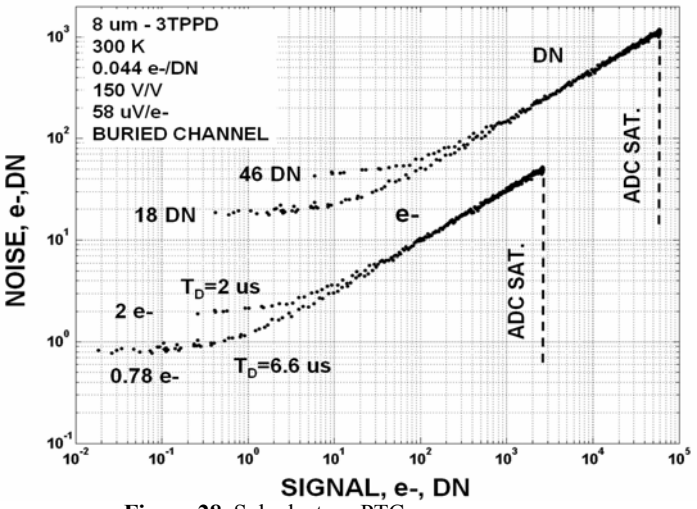

Figure 28. Sub electron PTCs.

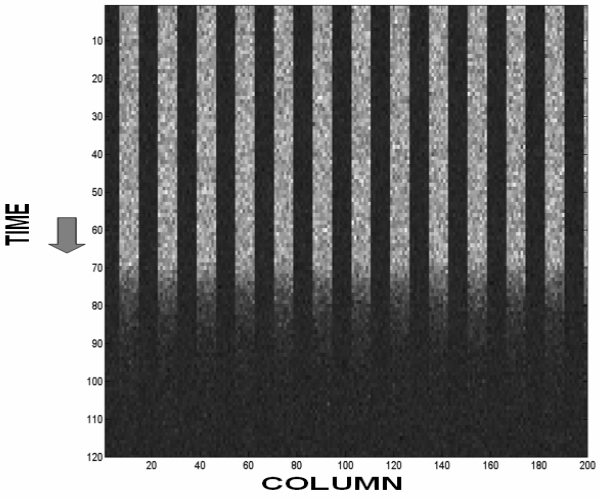

Figure 29. Ultra low light level square- wave image.

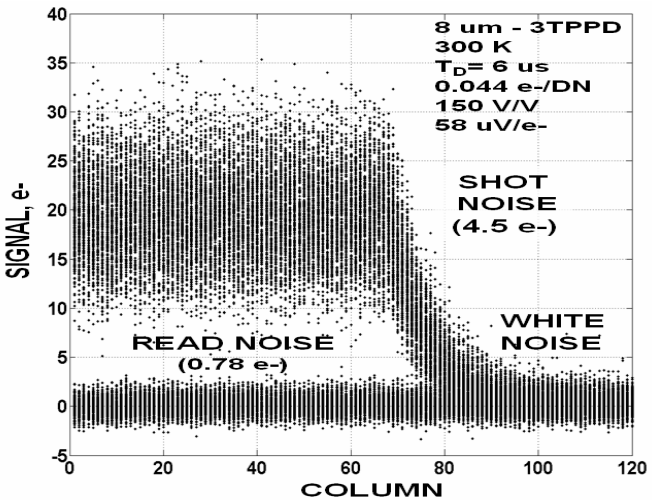

Figure 30. Stacked column noise plots for Fig. 29.

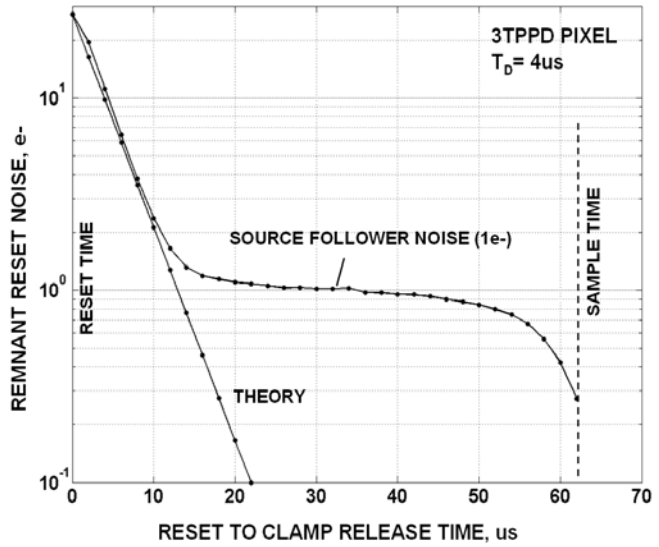

Figure 31. Remnant reset noise characteristics.

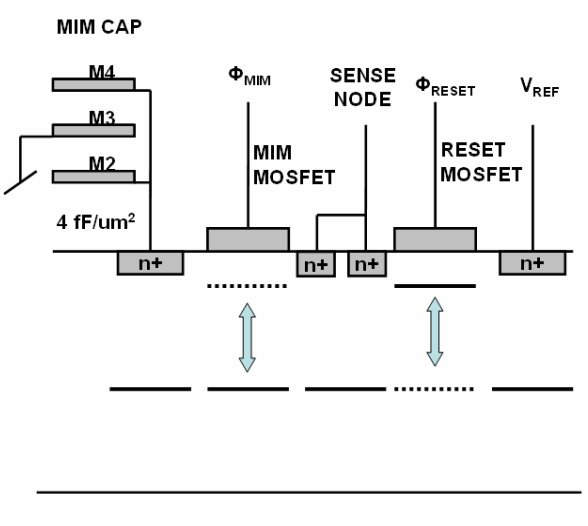

Figure 32. Parallel MIM pixel layout.

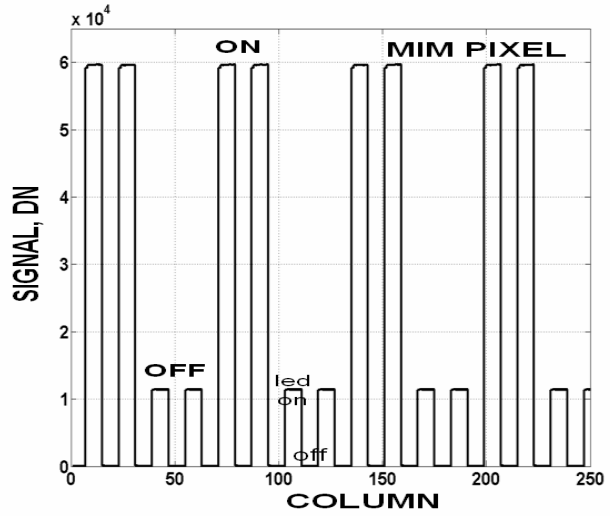

Figure 33. MIM pixel response for two gain states.

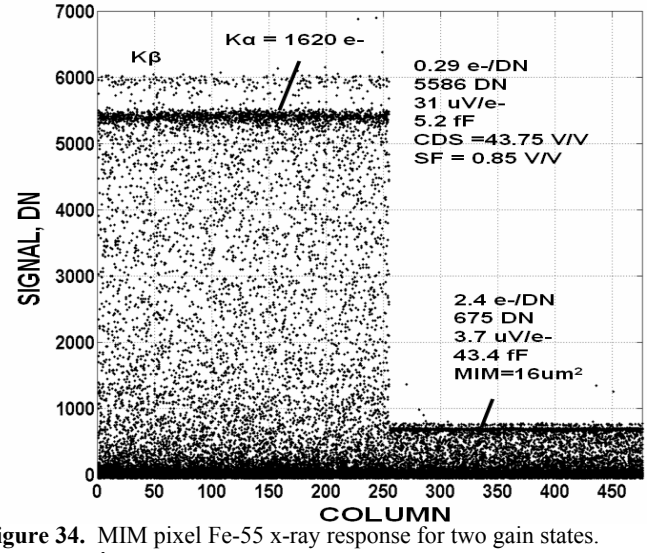

Figure 34. MIM pixel Fe-55 x-ray response for two gain states.

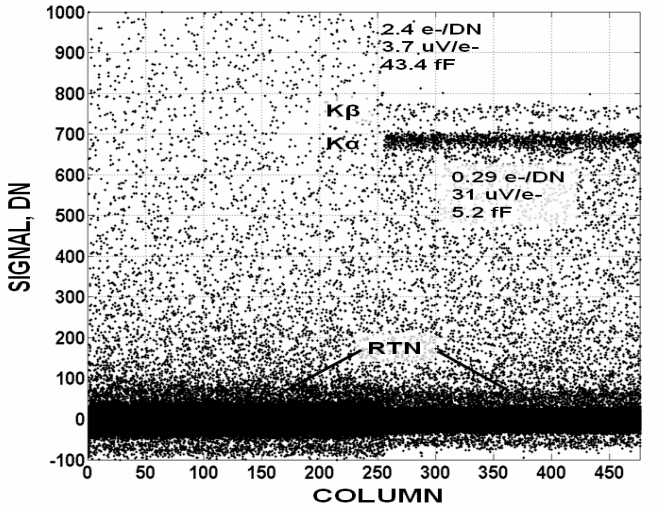

Figure 35. Magnified plot of Fig. 34 showing noise floors.

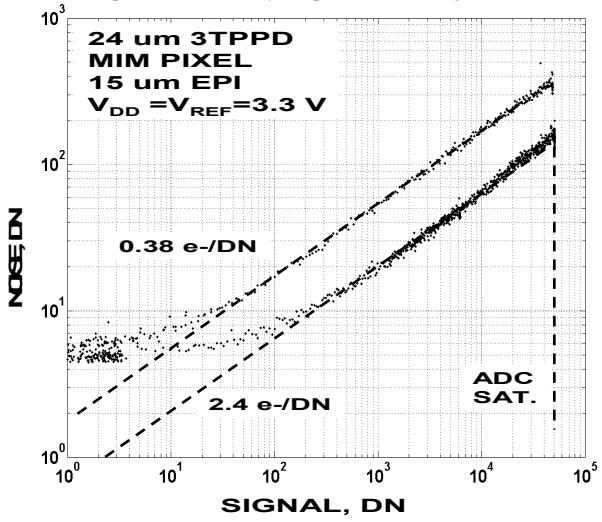

Figure 36. MIM pixel PTC (DN) for two gain states.

diffusion capacitance inherent with the parallel design significantly lowers sensitivity for the high gain state. It should be mentioned that the series arrangement requires a MIM driver for each row compared to a single driver used for the 'parallel' circuit in Fig. 32. The reset and MIM drivers can share the same drive voltages.

The MIM MOSFET is usually switched occasionally depending on how lighting conditions change. Sub frame MIM gain switching (e.g., row to row) is also possible using the series MIM configuration shown in Fig. 25a . It is also possible to extend the dynamic range (EDR) of the imager by double sampling a pixel in each gain state and storing the two results in a computer. However, this feature requires a complex clock timing sequence. The first sample must be taken in the high gain state before charge can be transferred to sense node or low noise performance will not be achieved. However, for large signals the sense node saturates in this gain state which results in incomplete transfer (i.e., charge is left behind in the PPD region after transfer). The deferred charge can be recovered by switching to the low gain state and clocking TG a second time followed by another sample to measure the high signal level.

The fill factor for the MIM pixel is compromised for frontside illuminated imagers since three metal layers above the pixel are required to form the MIM capacitor. However, for RING pixel the MIM capacitor can also act as a light shield required to block light from coming into the sense node region. For 3TPPD pixels an alternate implementation scheme without any fill factor loss involves controlling the diode depletion capacitance.[4] For example, Fig. 40 shows a PTC generated by a 16 um 3TPPD pixel fabricated on a custom 5 V /0.18um CMOS process. Note that high V/e- gain for low signals is produced when the PPD is fully depleted. At approximately 22,500 e- the PPD leaves depletion resulting in a dramatic increase in sense capacitance and gain decrease by a factor of 33 (50 /1.5). The signal compression technique produces a charge capacity of >3.25 x 10^6 e- set by the saturation level of the ADC (pixel full well is actually greater). However, the response is highly V/e- nonlinear within the gain change transition region. The signal level where the gain begins to change is controlled by the reset voltage, V_{REF} and the PPD implants used to fabricate the pixel. Figure 41 shows transfer characteristics of the pixel by plotting signal versus integration time.

7. 5TPPD RING PIXEL

The RING CMOS pixel was invented for large 5TPPD pixels required to transfer charge quickly and its ability to accept substrate bias more easily (refer to Fig. 42).[1] Figure 43 presents photon transfer data generated by a 256 x 256 x 16 um 5TPPD RING pixel imager demonstrating well behaved performance. The gain of the aCDS signal chain is such that the 16-bit ADC saturates before the pixel does. A lower gain setting shows that the pixel has an actual charge capacity of 70,000 e- that is limited by the sense node voltage swing (PPD full well is considerably higher). Read noise is 5 e- (assuming T_D=2 us) which translates to a dynamic range of 14,000 (82 db) for the sensor. A series MIM capacitor and switch are being added for the pixel in Sandbox VI to extend the dynamic range further.

Figure 43 shows that the sensitivity (V/e-) for the RING pixel is approximately half that of the 8um 5TPPD BIG MIN I pixel discussed above (i.e., 30 uV/e- versus 66 uV/e-). The low sensitivity measured is primarily governed by excessive TG to n+ sense node overlap capacitance (refer to Fig.42). New RING pixel designs are being fabricated on Sandbox VI to reduce the capacitance by moving the sense node n+ floating diffusion slightly away from the TG. Nonetheless, it is unlikely that the RING pixel will ever achieve high sensitivity as good as a conventional pixel design that BIG MIN I uses where a much smaller TG is employed.

Sandbox VI (Fig. 110) includes conventional 16 and 24 um 5TPPD pixel designs to achieve the same sensitivity as BIG MIN I. However, unlike the RING pixel where charge is transferred from all directions to a central sense node, charge for the conventional architecture must nearly transfer the entire diagonal length of the pixel to reach the sense node. This difference can be a potential speed issue for BIG MIN I pixel designs when minimum transfer time is required. Fortunately, PISCES simulations show that complete charge transfer can in theory take place in 1 micro-sec for a large 24 um pixel size. Future tests on Sandbox VI will verify this claim. Figure 44 shows a PTC 24 um 5TPPD RING pixel. Charge capacity and read noise are identical to the 16 um pixel using a TG clock width of only 100 ns.

Figure 45 presents low-light level CTE data for a 16 um RING pixel using a TG clock width of 100 ns. The top trace covers a signal range of 0 - 600 e- while the middle and lower traces cover 0 - 60 e- and 0 - 6 e- levels respectively. Deferred charge (image lag) is not present in all three traces with one electron measurement accuracy. Figures 46 and 47 shows Fe-55 x-ray stacking and histogram responses taken from 16 um 5TPPD RING pixels that demonstrate ideal

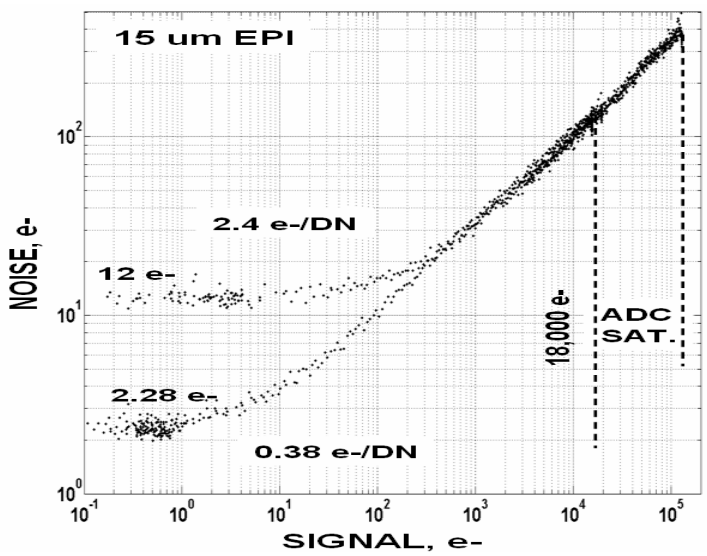

Figure 37. MIM pixel PTC (e-) for two gain states.

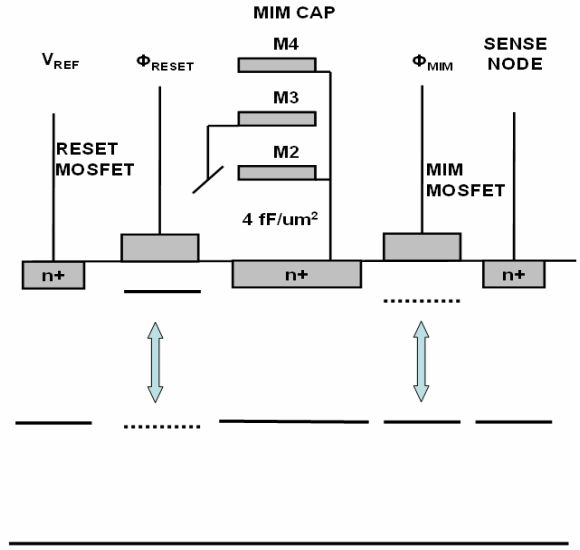

Figure 38. Series MIM pixel layout for lower noise.

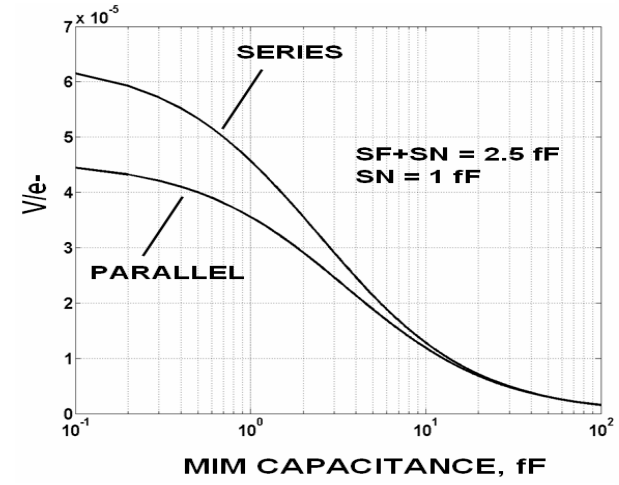

Figure 39. Parallel and series V/e- comparison.

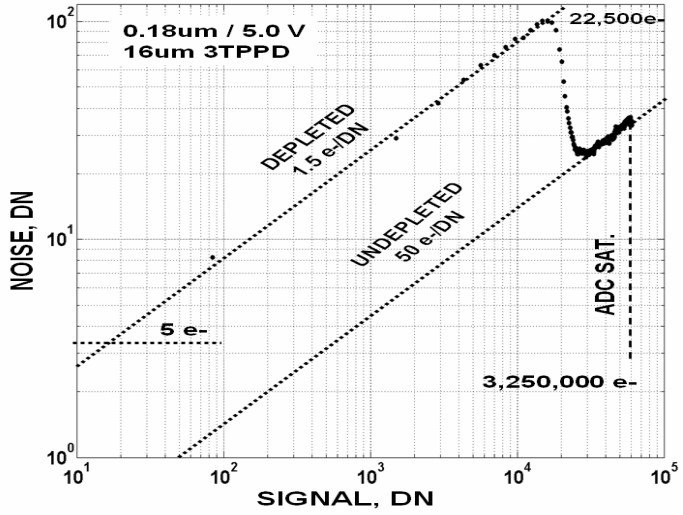

Figure 40. PTC for a two gain state 3TPPD pixel.

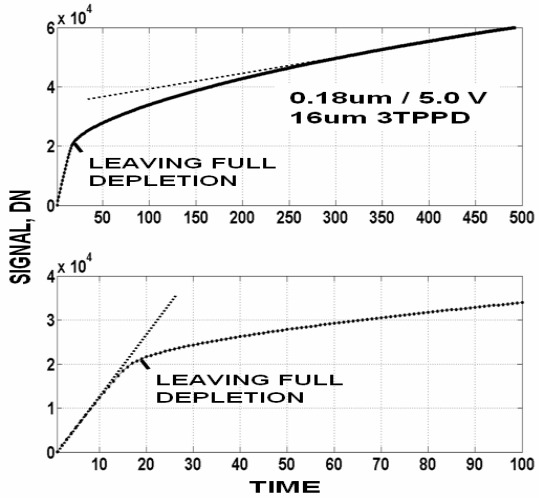

Figure 41. Transfer curves for a two gain state 3TPPD pixel.

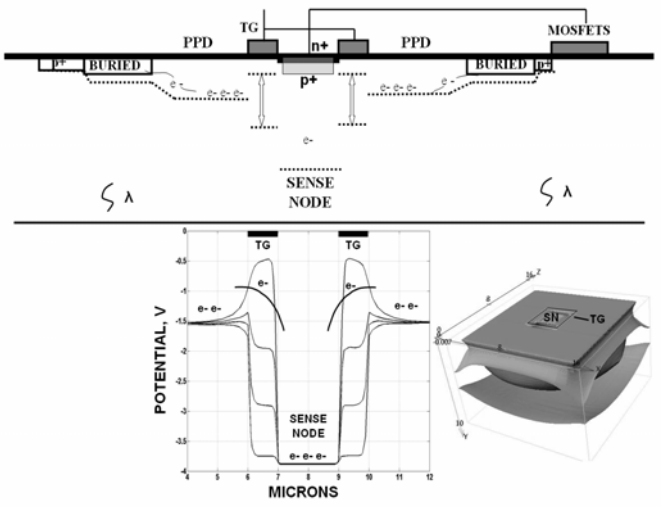

Figure 42. 5TPPD RING pixel.

absolute CTE performance. Figure 48 presents the x-ray stacking response as a function of TG clock voltage. Note that complete charge transfer without deferred charge takes place when TG >1.7 V. Figure 49 shows a CTE square-wave response that matches these results.

The x-ray histogram presented in Fig. 47 exhibits a very low partial x-ray event floor[6] indicating that charge splitting between the PPD and sense node region occurs very rarely. Figures 50 and 51 present PISCES simulations showing how electrons generated deep in the silicon naturally diffuse away from the sense node into the PPD region. Note that the deep carriers are initially attracted towards the sense node but are reflected away when they come within 3.0 um of the front side surface. At that distance the electric fields change polarity at the p-well interface thus forcing carriers to the PPD region. This action prevents partial x-ray event generation, improves charge collection efficiency (CCE) and quantum efficiency (QE) performance.

Figure 52 presents a Fe-55 x-ray row stacking plot for a 24 um 5TPPD RING pixel fabricated on 15 um high-resistivity (10,000 ohm-cm) epitaxial silicon. Note there are a significant number of split events generated indicating that the x-ray cloud of electrons occupies more than one pixel. For comparison, Fig. 53 is a Monte Carlo x-ray simulation showing various Fe-55 event charge cloud sizes with different diameters depending on how deep the x-ray photon interacts with the epi silicon (refer to Ref. 1 for simulation details). Although 24 um is sizeable pixel compared to the initial Fe-55 x-ray event cloud size (of approximately 1 um[6]) numerous split events are still created. The finite transit time required for deep charge clouds to reach the front side is responsible for the large sizes seen even though the 15 um epi silicon is fully depleted.[1]

Figures 54 and 55 present similar modeling results for 16 um 5TPPD and 8 um 3TPPD pixels with PPDs of V_{PPD} = 1V and V_{PPD} = 3.3 V respectively. For comparison, Figs. 56 and 57 show Fe-55 x-ray experimental images for both pixel sizes. The 16 um pixel is physically larger than the 8um pixel, and therefore assuming all variables were equal, should exhibit less charge splitting. However, the PPD depletion voltage for the 5TPPD is less than the 3TPPD pixel producing a cloud transit time that is three times greater than the 8 um 3TPPD pixel. In turn, the amount of diffusion and resultant charge cloud size is $3^{0.5}$ times greater.[1] Nevertheless, the larger physical size dominates with less charge splitting for the 16 um pixel as observed in the figures. CCE performance can be improved by using substrate bias (refer to Sec. 10 below). However, x-ray testing using substrate bias has not been performed to date.

Figures 53-55 clearly shows that target pixel area is an important factor in collecting signal carriers. It should be mentioned that depletion depth is also a function of PPD area (in addition to epi resisitivity / thickness, PPD potential and substrate bias). Figure 58 shows depletion depth contours as a function of PPD size assuming a circular PPD region where depletion depth is defined when 50 % of the boron atoms within the epi layer are ionized. Note that the depletion depth is shallow for a small PPD area and increases with PPD size to a fixed depth of 10 um (the assumed epi thickness with the immediate backside surface at ground potential). Ideally depletion depth is determined by the number of epi boron atoms ionized which is equal to the number of ionized phosphorus atoms within the diode region. However, for a small PPD area larger percentage of ionization takes place within the surrounding p-well region reducing vertical depletion. As the PPD size increases, both the depletion depth and volume increase.

Figure 59 shows a 'slant bar' response for a 24 um RING pixel. The imager test set up is illustrated in Fig. 60 showing a region of on-chip aluminized opaque pixels that form the slant bar. The light shield is designed at a slight tilt across one row of pixels to form the slant bar as shown. For this test the sensor is exposed to a diffuse light source at a wavelength of 9000 A for deep photon interaction. Responses are taken for row numbers 1-4 indicated with the slant bar over row-2. Note that row-2 exhibits nearly a perfect response with little pixel cross talk to rows 1 or 3 even though the light source is diffuse instead of collimated. Figure 61 presents a slant bar response for a 16 um RING pixel showing slightly more cross talk.

Figure 62 measures optical fixed pattern noise (FPN) for a 16 um 5TPPD RING pixel array in response to 9000 A light. The raw data shown is first flattened to remove non uniformity generated by the light source. Several rows are averaged together to remove photon shot noise. The flattened data that results shows optical FPN of 0.537 % of the average signal for the pixels.

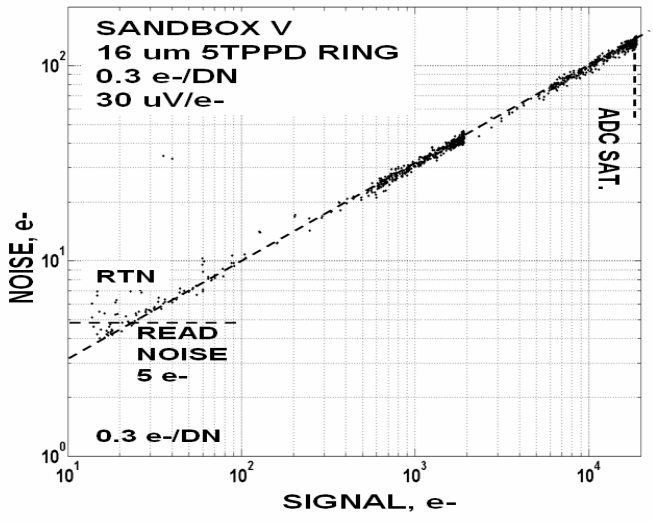

Figure 43. 16 um 5TPPD RING pixel PTC.

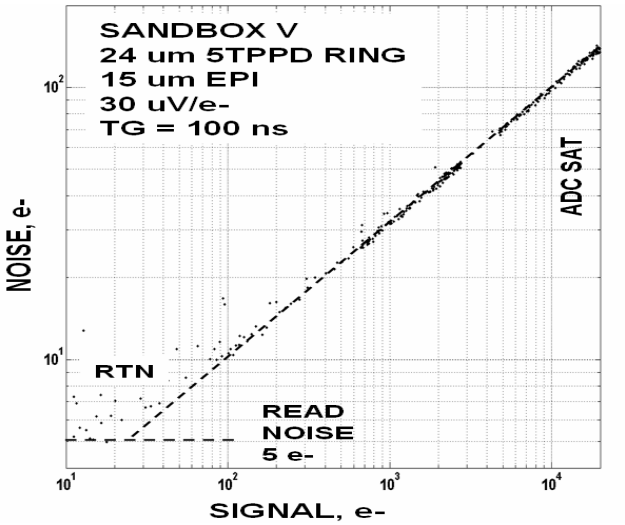

Figure 44. 24 um 5TPPD RING pixel PTC.

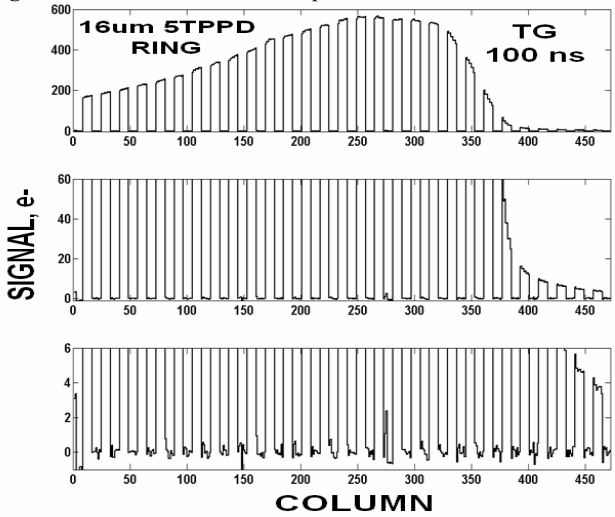

Figure 45. CTE response for a 16 um 5TPPD RING pixel**.**

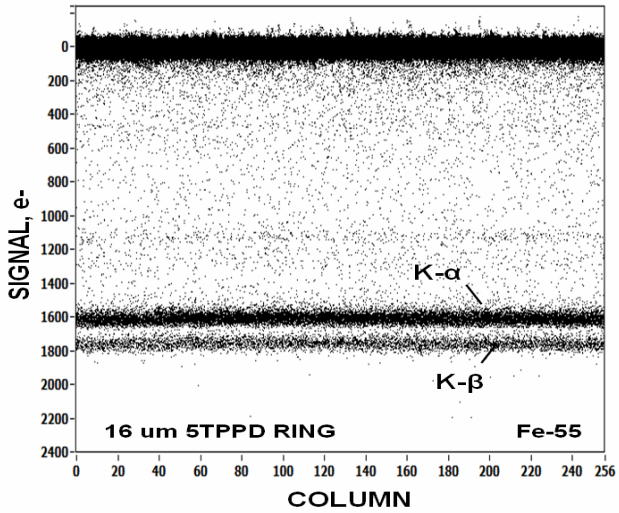

Figure 46. Fe-55 response for a 16 um 5TPPD pixel.

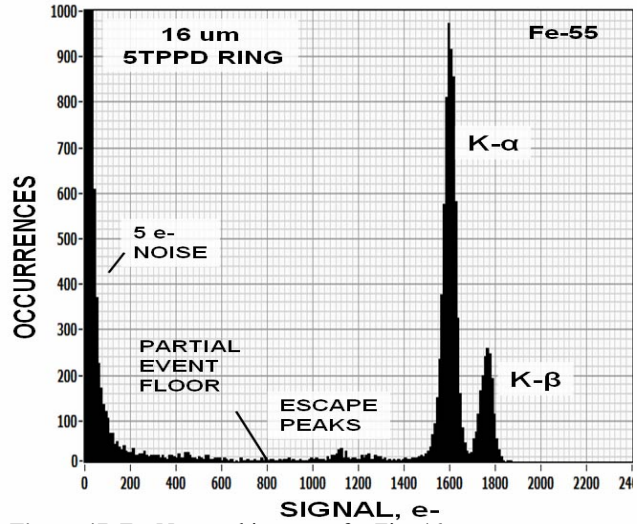

Figure 47. Fe-55 x-ray histogram for Fig. 46.

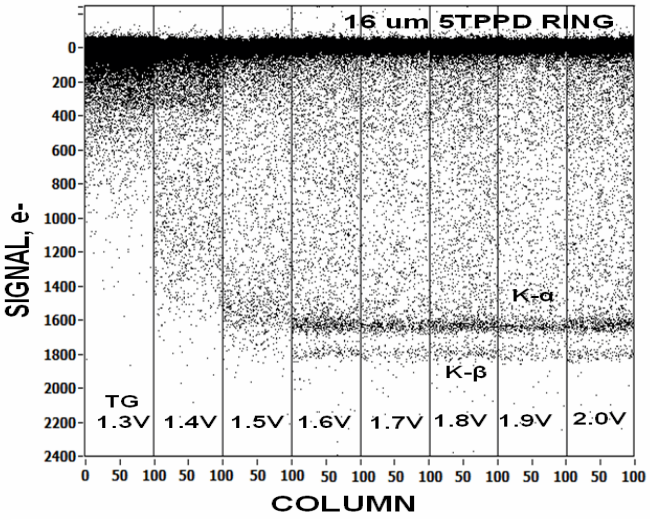

Figure 48. Fe-55 response as TG clock voltage is varied.

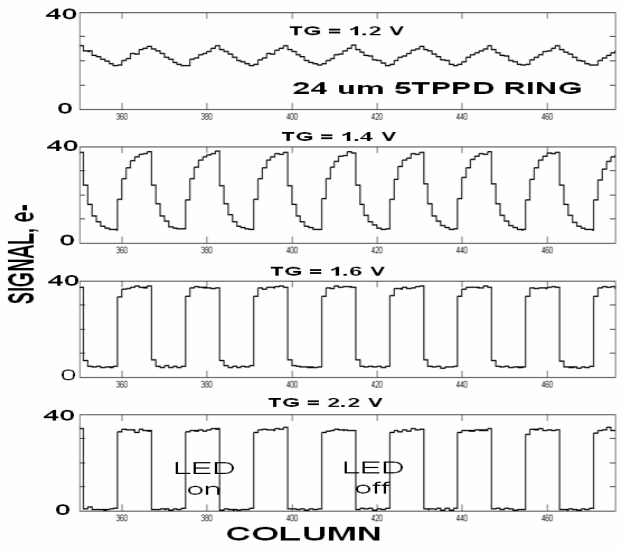

Figure 49. CTE response with TG clock voltage.

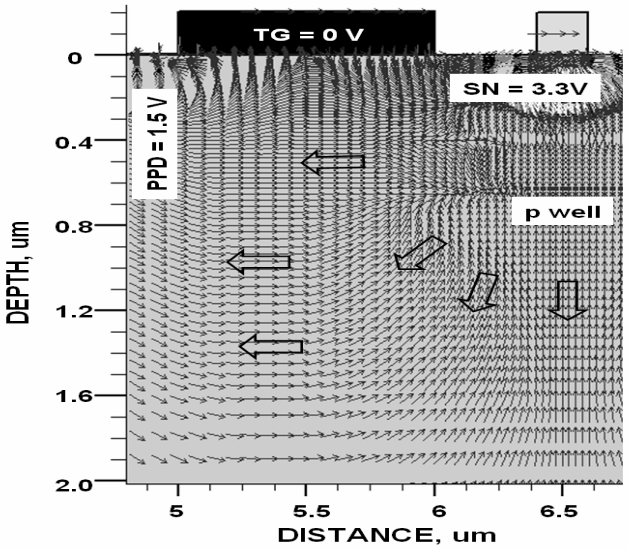

Figure 50. Simulation showing SN repulsion of carriers.

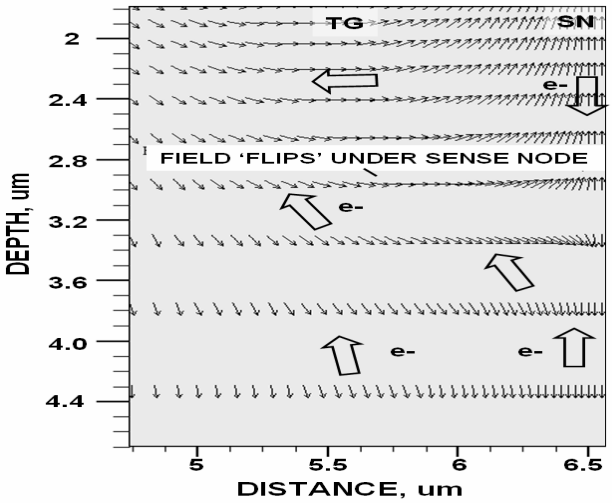

Figure 51. Magnified view of Fig. 50.

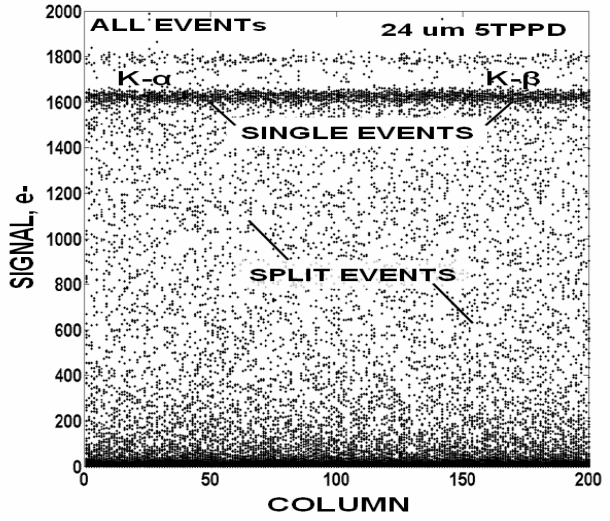

Figure 52. Fe-55 response for a 24um 5TPPD pixel.

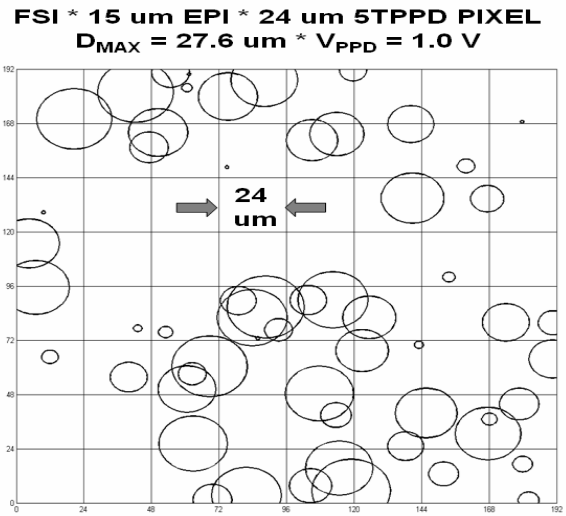

Figure 53. 24 um pixel Fe-55 simulation.

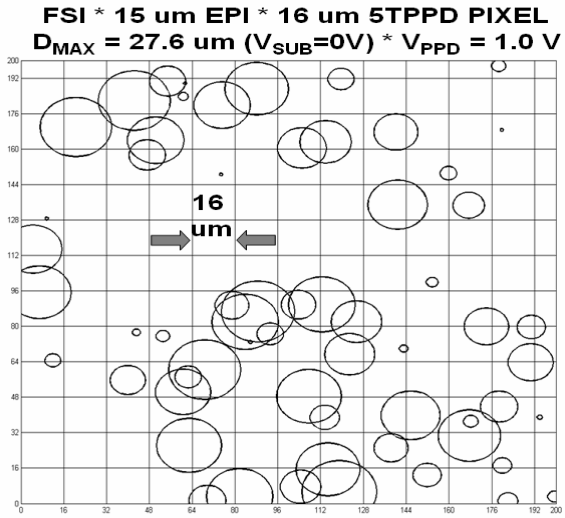

Figure 54. 16 um pixel Fe-55 simulation.

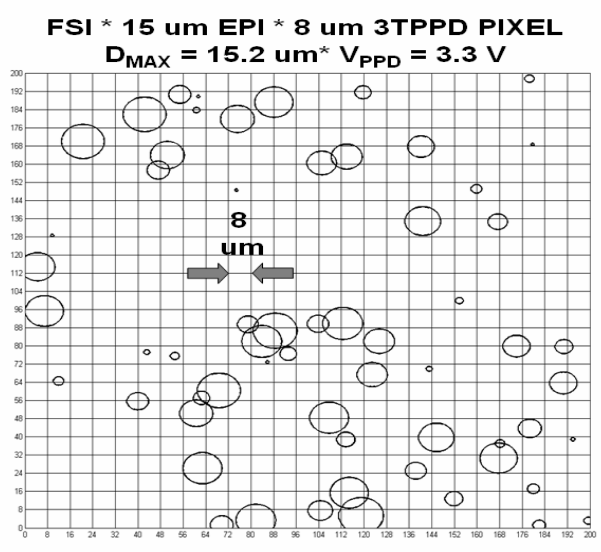

Figure 55. 8 um pixel Fe-55 simulation.

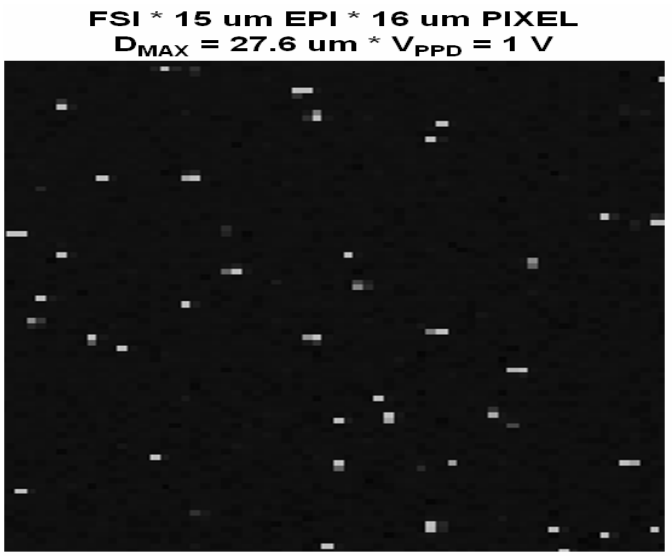

Figure 56. 16 um pixel Fe-55 image.

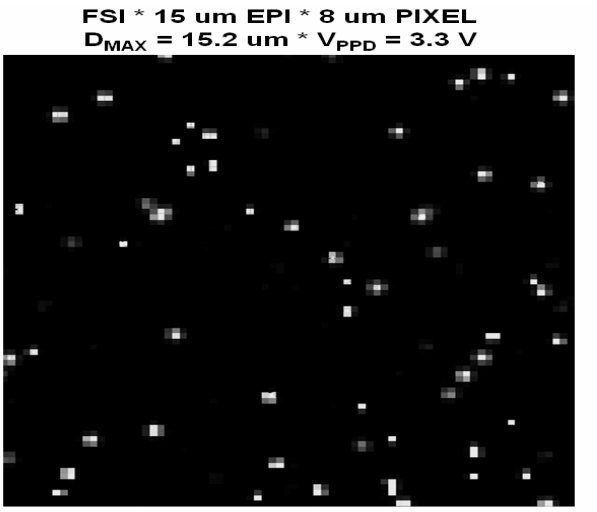

Figure 57. 8 um pixel Fe-55 image.

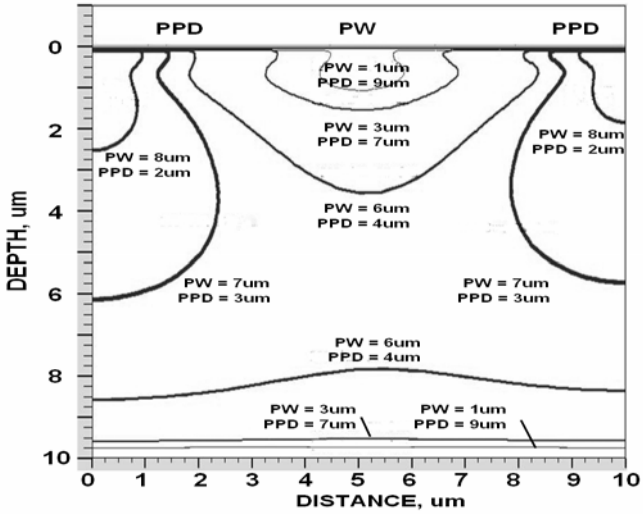

Figure 58. Depletion depth versus PPD size.

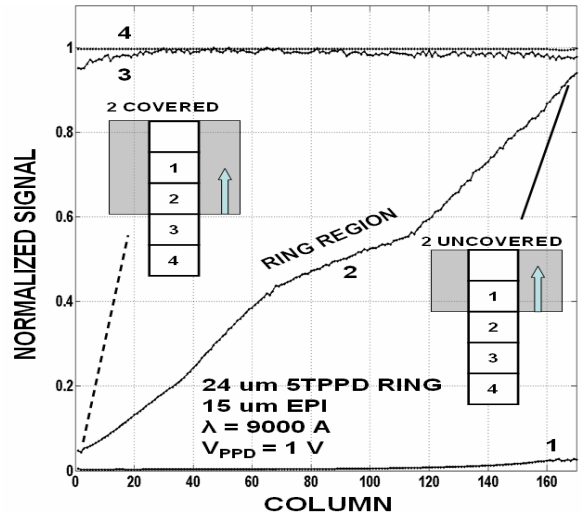

Figure 59. Slant bar response for a 24 um RING pixel.

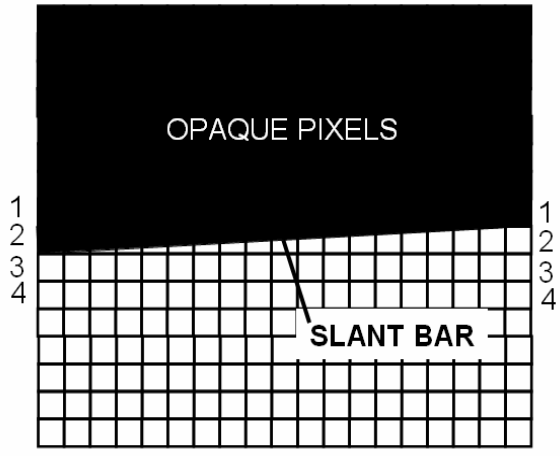

Figure 60. Slant bar pixel geometry for Fig. 59.

8. PIXEL BLOOMING

For maximum fill factor and low pixel cross talk it is desirable to have the p-well barrier regions between pixels as narrow as possible. However, if the p-well width is made too small pixel-to-pixel blooming will arise. Figure 63 plots the maximum potential through the PPD and p-well regions as a function of signal level. Note at zero signal a respectable potential exists under the barrier although the PPD potential is still greater to collect charge. As signal increases the barrier and PPD potentials decrease together. Charge spills over into neighboring pixels when the potential difference between the barrier and PPD regions is approximately 0.5 V (via kT). The p-well width that is actually employed depends on pixel architecture, silicon resistivity and processing details.

Pixel blooming is usually not observed for CMOS pixels because excess charge can usually escape through drains located within the pixel. For example, in the case of 3TPPD bloomed charge can find its way through the reset MOSFET as long as the surface potential under the reset gate is less than the pixel p-well barrier potential. Figure 64 plots signal generated by a 3TPPD pixel as the low level, $V_{\Phi PCL}$, of reset clock is increased. Note when $V_{\Phi PCL}$ = 0V that pixel-to-pixel blooming occurs indicating the p-well barrier is insufficient to hold back charge. Increasing $V_{\Phi PCL}$ to 1.0 V stops blooming signifying that excess charge is draining through the reset MOSFET. Between $1.0 < V_{\Phi PCL} < 2.0$ V pixel full well is limited by the source follower MOSFET saturation. Increasing $V_{\Phi PCL}$ beyond 2.0 V lowers the dynamic range due to blooming through the reset MOSFET.

Pixel blooming for a 5TPDD pixel shown in Fig. 65 takes place when excess PPD charge can't escape through the transfer gates (TG1 and TG2). However, when TG1/TG2 clock potentials are less than the p-well barrier charge will bloom into the sense node region. Once there, the low level of the reset ($V_{\Phi PCL}$) can be adjusted to remove excess charge as discussed above. TG2 is usually used to prevent pixel-to-pixel and PPD to sense node blooming with the latter a common problem for global shutter (SNAP) applications. For example, Fig. 66 shows video row traces taken from a 5TPPD RING pixel as TG2 clock voltage is increased. Note the charge level that can be contained in the PPD region decreases with TG2 voltage with significant variation from pixel to pixel.

9. BURIED CHANNEL PHOTOGATE AND CMOSCCD

Sandbox VA (5.0 V) included different CMOS buried channel photo gate (PG) pixels and a 128(V) x 512(H) x 8um CMOS CCD imager.[1] Initial test results are reported here, however, more detailed characterization will take place after this paper is submitted. Relative to the PPD pixel, the buried channel PG pixel shown in Fig. 67 has special performance strengths that are advantageous to specific imaging applications. However, the main purpose for the PG pixel at this time supports advanced development of the CMOSCCD. Figure 68 shows CTE square-wave test results generated by an 8um PG pixel that is fully buried channel including TG1, TG2 and sense node. For comparison, data generated for the same PG pixel design without the custom buried channel implant is also presented. As can be seen, CTE performance for the buried channel pixel is superior given that surface state trapping under the PG does not take place.

Figure 69 presents PISCES simulation for a buried channel PG pixel that plots PG, TG1 and sense node potentials at different PG drive voltages with TG1 fixed at 0 V. The plot shows that charge can be transferred by only clocking PG. However, to overcome charge traps that might be present it is best to clock both PG and TG using the timing diagram shown in Fig. 67. Figure 70 is data showing the relationship of the sense node (V_{REF}) to the low clock level of TG1 when no charge transfer takes place (i.e., TG1 and sense node potentials are equal). A TG1 threshold voltage of approximately 1.5 V is measured agreeing with simulation results.

As experienced during CCD development, optimum full well for the PG pixel depends on PG clock drive and buried channel implant details.[6] If the PG is overdriven the potential well under the PG will operate surface channel resulting in poor CTE performance (a saturation condition referred to 'surface full well' (SFW)). This problem is illustrated in Fig. 71 showing potential well shape as a function of PG drive voltage assuming TG1 = -2V. Note when PG is biased to 3.0 V the difference between the surface to channel potential is insufficient to keep signal carriers from interacting with the surface (at least 15 kT V is required to maintain surface isolation). However, as the PG voltage is lowered the surface barrier height increases thus improving charge capacity. However, if the PG is clocked too low an insufficient barrier between PG and TG1 potentials will result causing blooming into the sense node (referred to as 'bloomed full well'

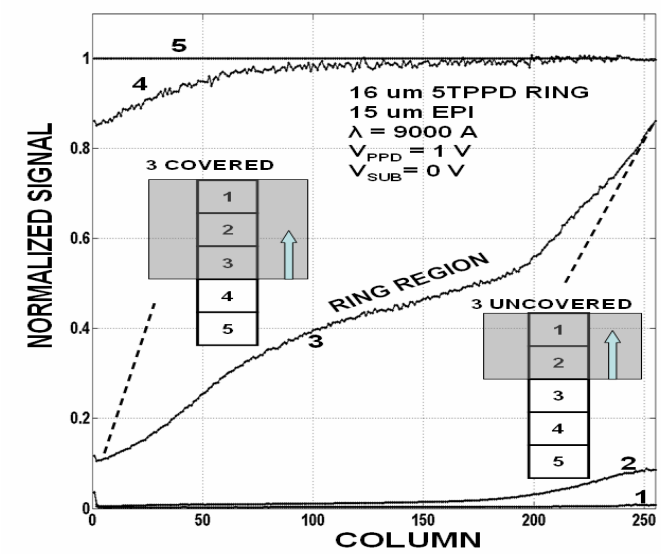

Figure 61. Slant bar response for a 16 um RING pixel.

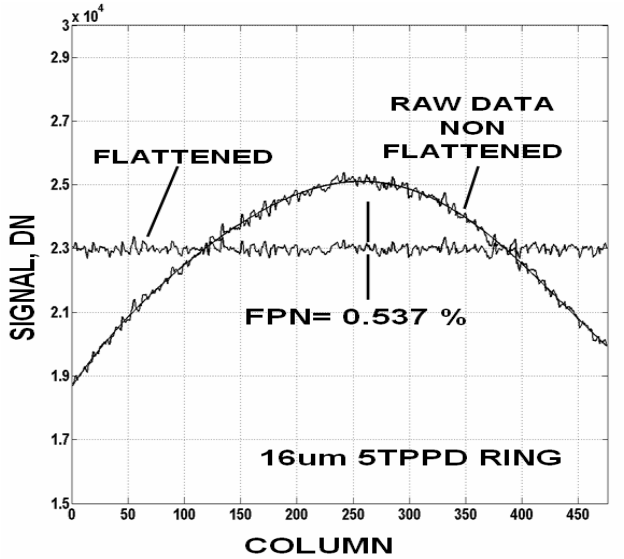

Figure 62. Optical FPN for a 16 um 5TPPD RING pixel.

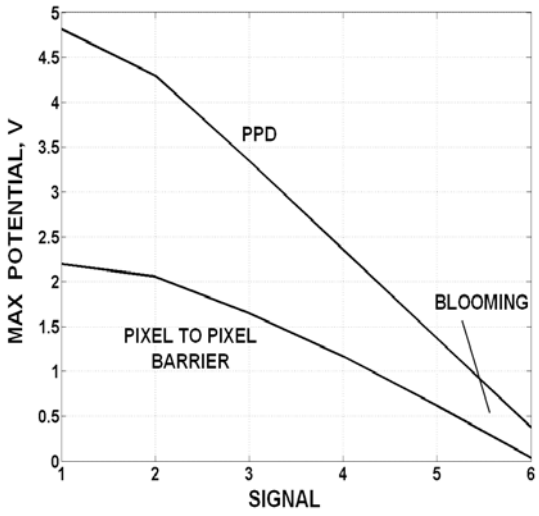

Figure 63. PPD and p-well potential with signal.

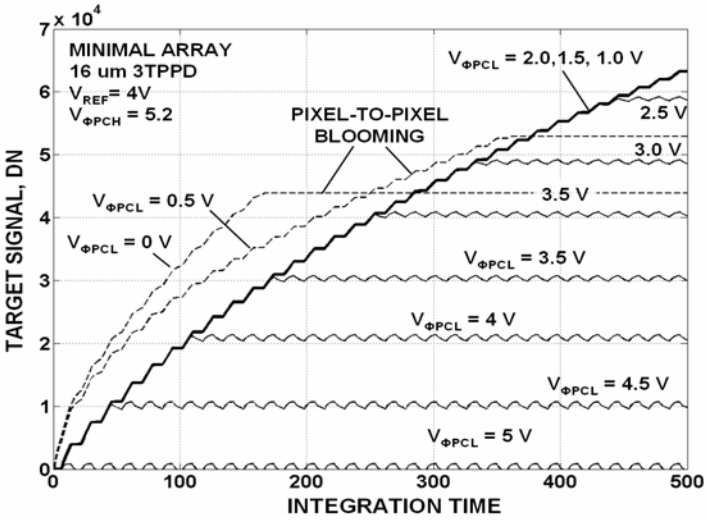

Figure 64. Pixel blooming characteristics for a 3TPPD pixel.

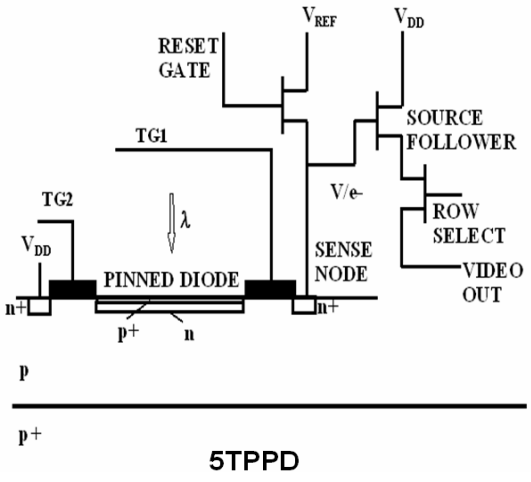

Figure 65. 5TPPD pixel schematic.

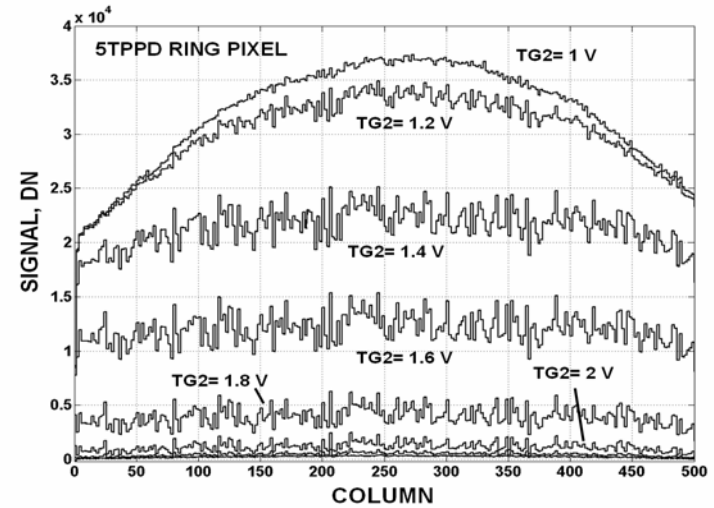

Figure 66. TG2 sense node anti blooming control.

(BFW)). Hence, there is a optimum PG voltage where charge capacity is maximum. This bias condition takes place when both BFW and SFW take place together (approximately PG=1 V in Fig. 71).

Figure 72 presents low signal level CTE square-wave data under two different drive conditions (PG = 1 V and 3.0 V) for a relatively small PG buried channel pixel. As can be seen, poor CTE performance is exhibited for a PG clock voltage of 3.0 V caused by surface state trapping. Charge capacity with good CTE is essentially zero under this bias condition. In contrast, running the PG clock at 1.0 V shows good CTE and some charge capacity. Figure 73 presents a PTC with the PG clocked at 2 V. Note at approximately 25,000 DN (10,750 e-) the photon shot noise curve starts to deviate from a slope of ½ indicating that CTE performance is degrading as charge interacts with the surface (i.e., SFW has taken place). At a much higher light level, beyond SFW, the photo gate blooms over the TG barrier at 25,000 e- (i.e., BFW).

Buried channel PG pixel processing details can be extended to a four phase single poly CMOSCCD array.[1] Figure 74 presents potentials under the phases when they are clocked high and low with voltages indicated. Figure 75 shows potential well shapes for the collecting phase at different gate voltages. Note that a 3.0 V gate bias produces a surface to channel potential difference of 1 V for good SFW charge capacity. Figure 76 plots potential versus gate voltage for three different normalized buried channel implant energies (E_n=1, 0.75 and 0.5). Note that clocks can be taken into inversion with a gate voltage of -1V to reduce dark current and eliminate surface residual image.[6] However, excess charge (gate leakage) through the thin oxide may prevent this mode of operation depending on integration and frame readout times. Fortunately, residual image can be removed by briefly (micro-sec) taking the imager into inversion before an exposure is taken. CMOSCCD testing is currently taking place and will be reported in a subsequent paper (Part V).

It should be mentioned that Jazz/Tower Semiconductor offers 3.3 V and 5.0 V CMOS 0.18um processes as used by the imagers discussed above. However custom pixel implants required, such as buried channel, must be developed by the customer. Both processes have been employed to fabricate buried channel PG pixels and CMOSCCD imagers. The higher operating voltages offered by 5.0 V processing improves dynamic range and provides additional voltage margin to transfer charge from the CCD register onto the sense node. Also, the 5.0 V process provides a thicker gate oxide which significantly reduces gate leakage issues especially when CCD potential wells are biased into inversion. However, 5.0 V is a relatively new fabrication process compared to 3.3 V and additional lot runs are required to advance its maturity. Sandbox VC is the next 5.0 V run currently in fabrication (Fig. 109).

10. SUBSTRATE BIAS

Substrate bias was introduced in Ref. 1 as a general CMOS biasing technique to reduce carrier collection transit time and pixel cross talk. Preliminary experimental data from Sandbox V test arrays designed for substrate bias is presented in this section. As PISCES modeling showed previously the amount of substrate bias that can be applied to the imager is dependent on substrate bias (V_{SUB}), reset voltage (V_{REF}), PPD depletion voltage (V_{PPD}) and many specific pixel and array design variables. Figure 77 plots substrate bias current as a function of V_{SUB} and V_{REF} for a 16 um 3TPPD 20 (H) x 16 (V) 5.0 V processed test array with V_{PPD} = 4 V. Note for this imager operating voltages of V_{REF}= 3 V and V_{SUB}= -10 V can be used without significant substrate leakage current. In that V_{PPD} is solely determined by the PPD implants, the reset voltage V_{REF} controls substrate leakage. However, when V_{REF} reaches V_{PPD} it loses control which explains why the curves of Fig. 77 start to clump together at approximately 4 V.

Figure 78 presents a row of pixels taken from an image generated by a 512(H) x 496 (V) x 16 um 3TPPD Minimal Array. The imager is exposed to 9000 A light under two substrate bias conditions (V_{SUB} =0 and -6V). The rows of pixels above and below the target row plotted are kept in a constant 'hard reset' condition (V_{REF} = 4.5V). This setup condition represents a worst case pixel cross talk situation as signal charge generated deep in the epitaxial silicon is attracted more to the hard reset rows than the target row of pixels. This is because the target pixels contain charge thus reducing PPD potential and depletion depth where other rows without charge remain in the fully depleted state. Note when substrate bias is applied the target row attracts more charge indicating less charge is going to the hard reset rows. Increasing substrate voltage beyond -6V only shows a small CCE improvement showing that depletion depth is maximized for the array. Figure 79 shows a different row of pixels taken at a wavelength of 4300 A. In this case, the response is independent of substrate bias since blue photons are absorbed at the surface of the pixel where depletion depth is not important. Figure 80 plots substrate current as a function of substrate bias for the imager showing negligible substrate current at V_{SUB} = -6V.

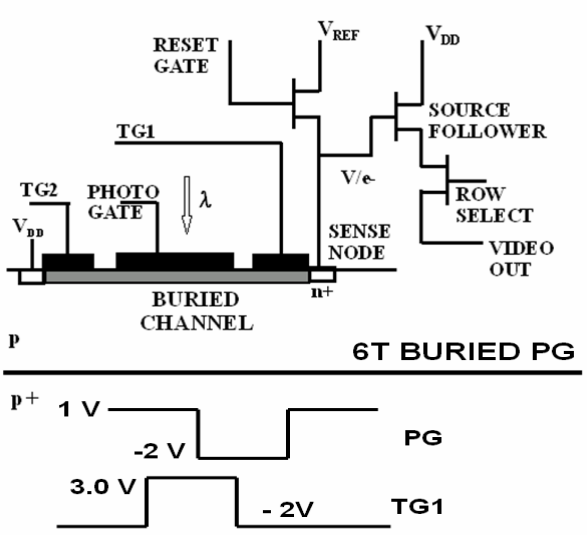

Figure 67. 6T buried channel CMOS PG pixel schematic.

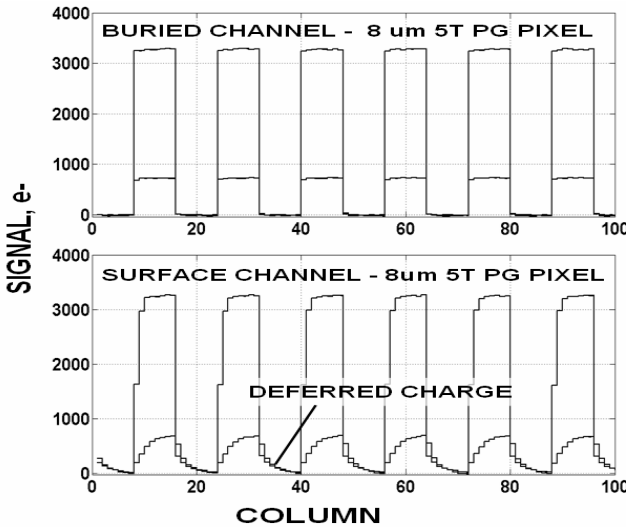

Figure 68. BC and SC PG CTE characteristics.

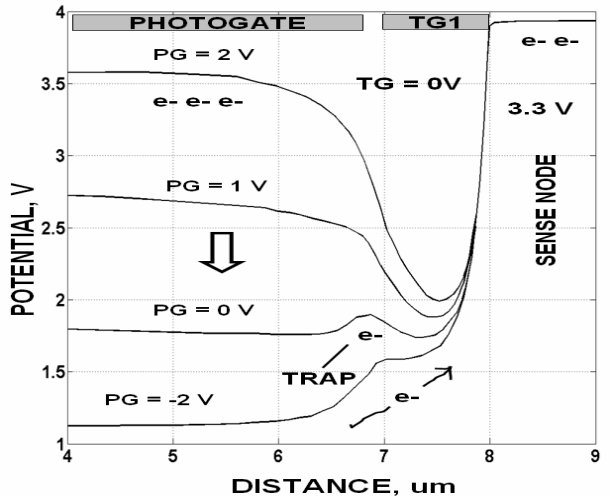

Figure 69. BC PG pixel potential profiles.

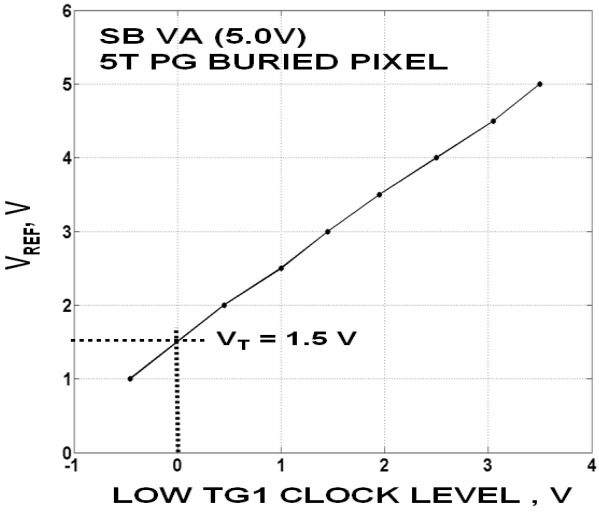

Figure 70. Measured TG1 potential.

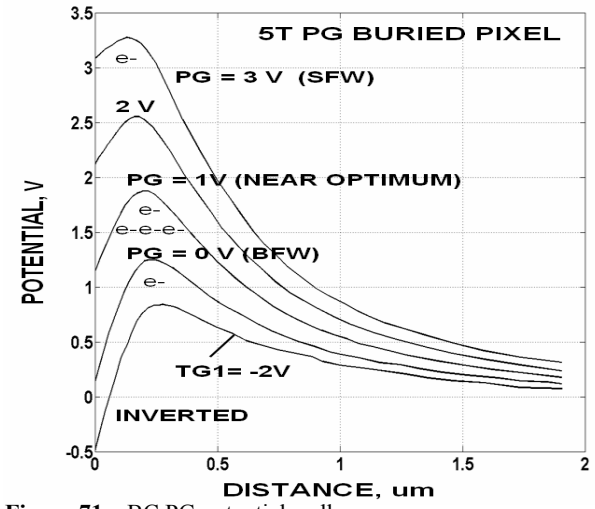

Figure 71. BC PG potential wells.

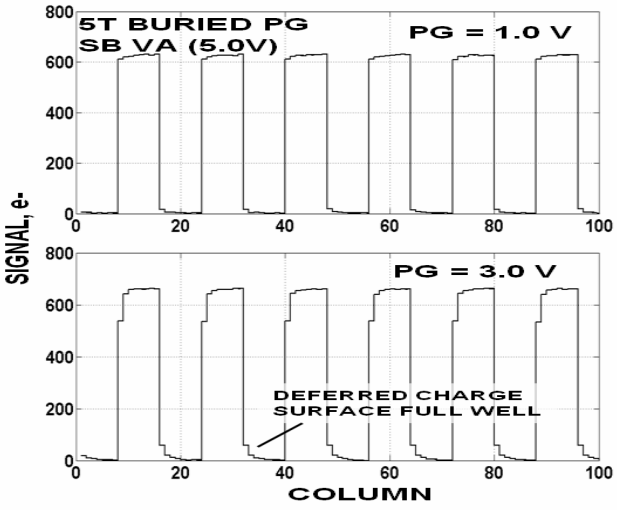

Figure 72. BC PG biased into the SFW condition.

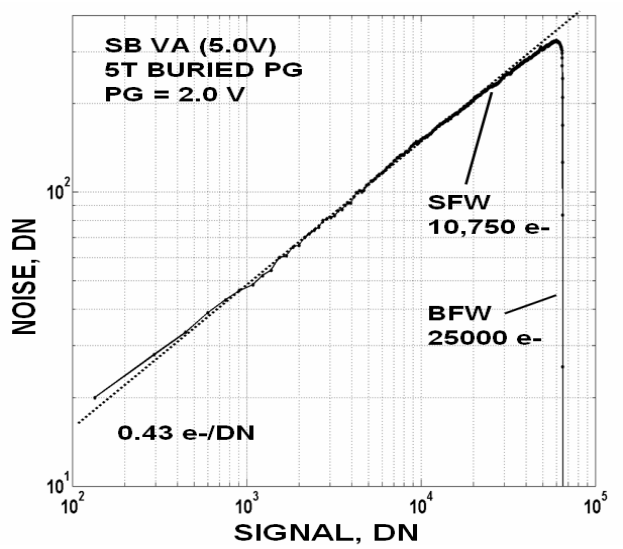

Figure 73. BC 5TPG PTC showing SFW condition.

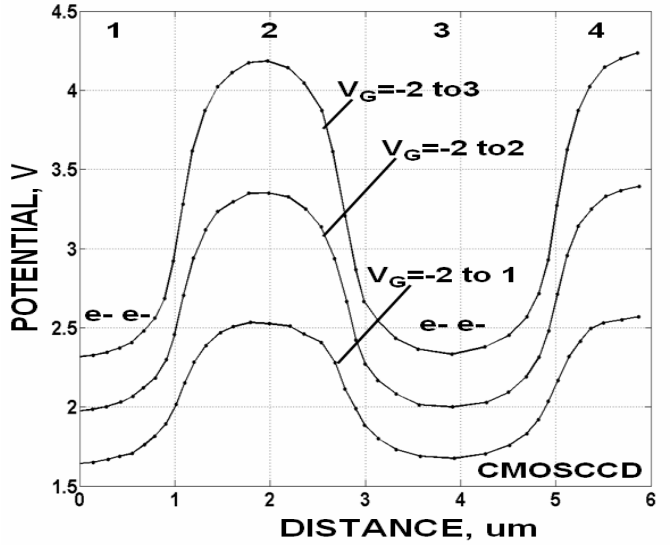

Figure 74. 4-phase CMOSCCD potentials for charge transfer.

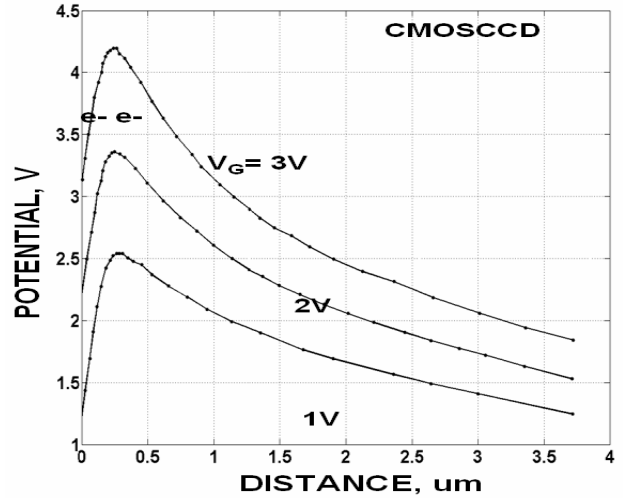

Figure 75. CMOSCCD potential wells.

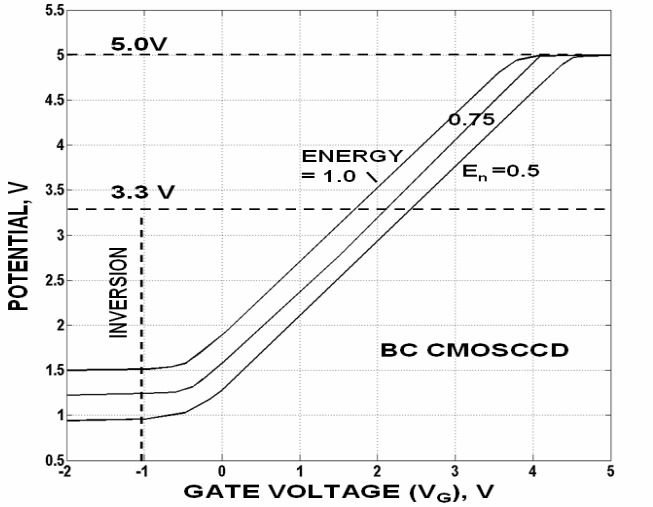

Figure 76. CMOSCCD channel potentials with different BC.

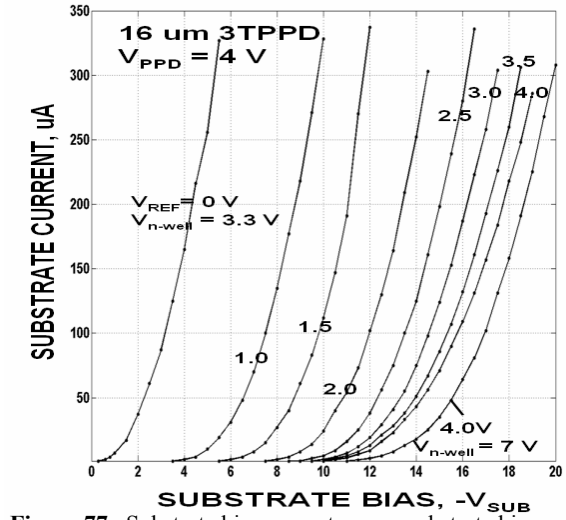

Figure 77. Substrate bias current versus substrate bias.

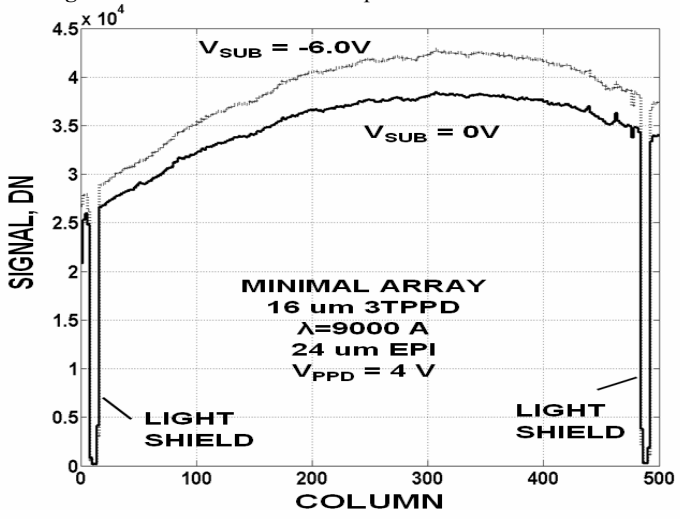

Figure 78. 9000 A image response to substrate bias.

The light shield on the right side of Figs. 78 and 79 is magnified in Fig. 81 showing blue and near IR responses together. For ideal pixel cross talk performance, no signal should be measured within the opaque region. This is the case for the 4300 A trace whereas the near IR response exhibits some cross talk and decreases as substrate voltage is applied.

Figure 82 shows responses from a single 16 um 3TPPD pixel taken from the imager of Fig. 78 integrating charge as a function of time for negative and positive substrate bias conditions. As before, rows above and below the pixel are kept in the hard reset condition. Note that for low signals substrate bias is not critical because the target pixel and surrounding neighboring pixels attract charge equally. However, as the signal level increases the target pixel relies more on substrate bias for good CCE. As substrate voltage goes positive more and more charge goes to neighboring pixels especially at high signal levels. Figure 83 shows the light shield region at all substrate bias conditions.

The substrate bias imagers characterized above are fabricated on 24 um high-resistivity (>10,000 ohm-cm) epitaxial silicon (refer to Fig. 84). The residual charge measured in the light shield region of Fig. 83 may come from charge generated deep within the auto doped tail and substrate regions (also some scattered light from the LED source may be present). Substrate bias is not effective in these regions because depleting low resistivity silicon is difficult and results in excessive substrate leakage current. Thinning can remove this neutral material to allow the depletion region to completely extend to the backside of the imager as indicated in Fig. 85.[1]

11. DARK SPIKES AND DARK CURRENT

11.1 Dark Spikes

Occasionally very 'hot pixels' associated with high leakage current generated on the sense node are observed (refer to Fig. 65 and 67). The problem is especially critical to the global shutter (SNAP) readout mode where signal charge must be stored on the sense node for the entire frame readout time. This readout situation is different than progressive scan where charge only needs to be on the sense node a very short time (i.e., aCDS process time that is approximately 10 us depending on read noise requirements). The dark spike issue is also important when the sense node voltage (V_{REF}) is elevated to enhance dynamic range as discussed below.

Figures 86 and 87 show 3D dark images taken by a 256 x 256 x 16 um 5TPPD imager that exhibits the sense node dark spike problem (representing a worse case sensor). Note there are considerably more spikes when the sense node is reset to V_{REF} = 4.0 V compared to 2.0 V bias indicating that the charge generation rate is electric field dependent. Figure 88 collectively shows the dark spikes and amplitudes as a function of V_{REF}. Figure 89 shows selected spikes as a function of charge integration time. Note that signal increases nonlinearly until charge generation rate decreases significantly at a specific signal level. Figures 90, 91 and 92 show how the spikes respond to operating temperature assuming an integration time of 5.4 sec as the rows are read progressively. At warm operating temperatures the dark spikes mix with thermally generated dark current from TG and bulk epitaxial silicon regions (as discussed in Sec. 11.2 below). Epi dark current decreases at the expected rate with temperature (i.e., approximately 2x reduction for a 7 C degree change). However, the spikes are stubborn and require additional cooling to suppress their presence. Figure 93 shows average global sense node leakage current generated for a single row of pixels without high level dark spikes. Characteristics are similar to the spikes where dark current is also dependent on V_{REF} bias.

The data collected above shows that spike leakage is characteristically different than thermally generated silicon dark current. Noting that the spikes are dependent on V_{REF} (and associated fields) implies the problem is connected to the n+ sense node floating diffusion. A weak form of 'contact metal spiking' for pixels with spikes may explain the leakage problem. This implies that the n-p junction may not be deep enough for the contact metallization processes commonly used for non imager applications. Following this theory, Figures 94 and 95 show a row of 3TPPD pixels and corresponding dark image for a test pixel array that is processed with a shallow contact (labeled as Contact-A). Note that nearly every pixel is a hot pixel in the breakdown condition. In comparison, a much improved dark response is also shown in Fig. 94 that uses a deeper contact without spikes (Contact-B).

Upcoming Sandbox runs planned will attempt to improve consistency and reliability for the sense node contact. Motivation is high since it has already been demonstrated that very low contact dark current without spikes is possible (from earlier work accomplished using a 0.25um process). For example, the top plot of Fig. 96 shows the sense node dark current generated for several 3TPPD pixels fabricated using a custom contact. Note that pixels generate <700 e-/sec

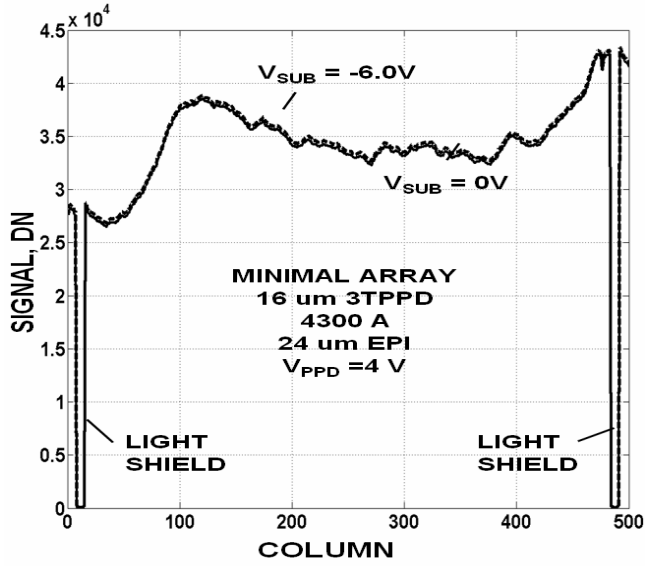

Figure 79. 4300 A image response to substrate bias.

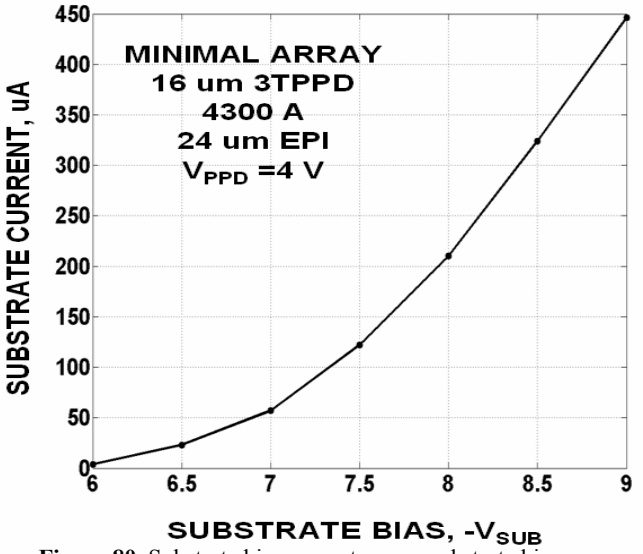

Figure 80. Substrate bias current versus substrate bias.

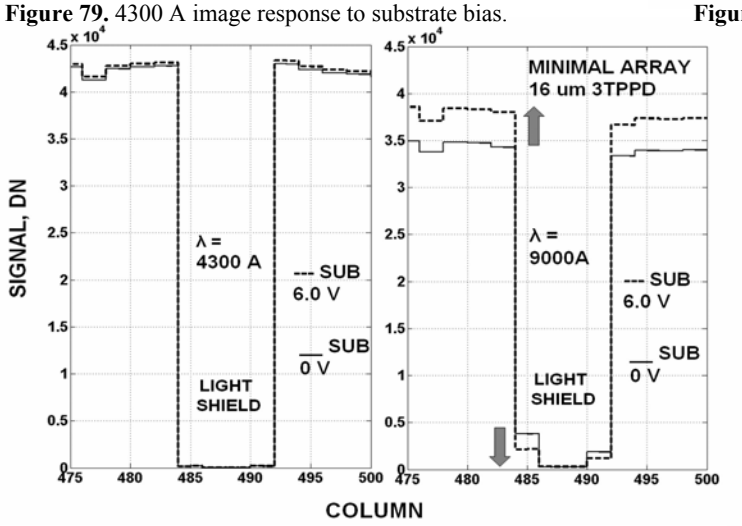

Figure 81. Edge 4300 and 9000 A responses to substrate bias.

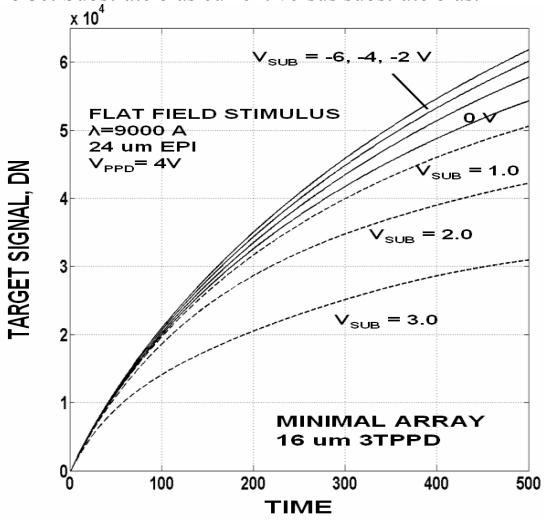

Figure 82. Substrate bias response with signal.

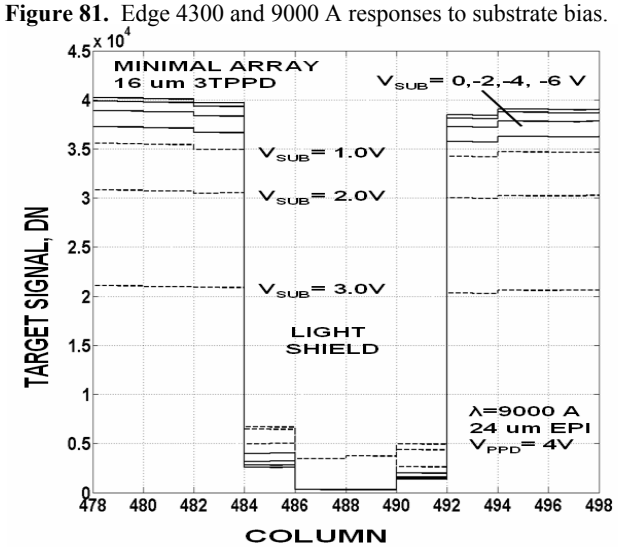

Figure 83. Edge responses for Fig. 82.

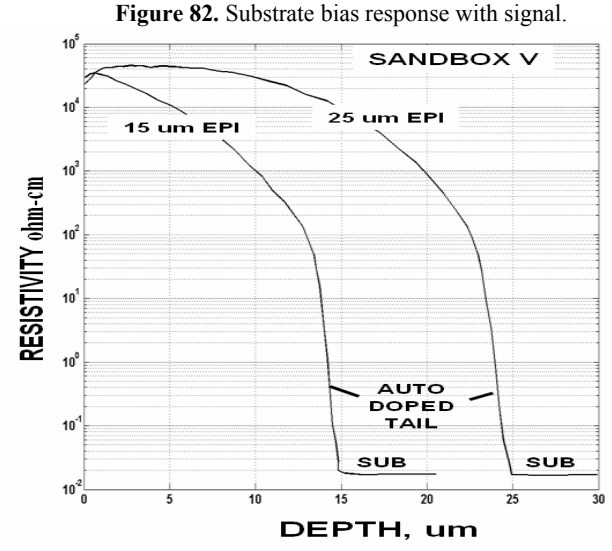

Figure 84. Silicon resisitivity for 15 um and 25 um epi.

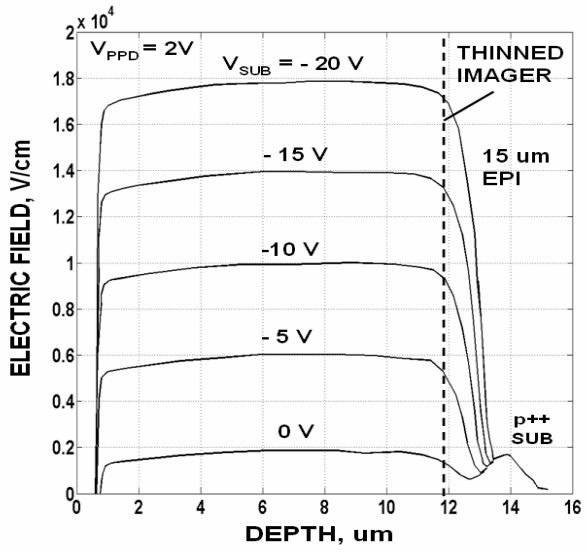

Figure 85. Electric fields with substrate bias for Fig. 84.

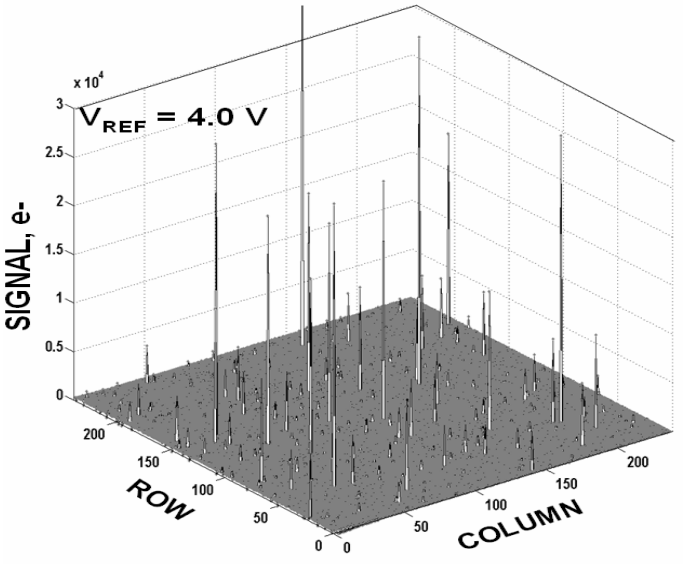

Figure 86. Sense node spikes at V_{REF}=4.0 V.

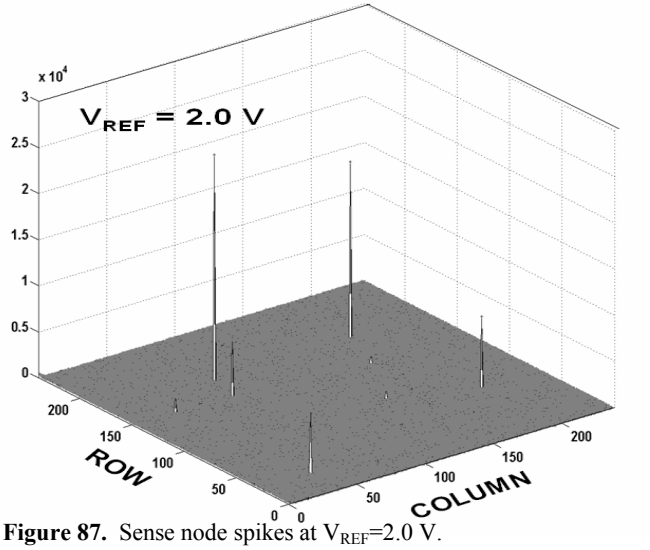

Figure 87. Sense node spikes at V_{REF}=2.0 V.

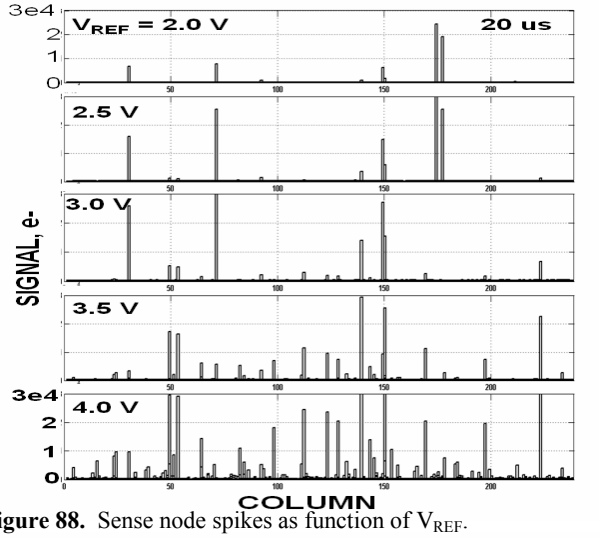

Figure 88. Sense node spikes as function of V_{REF}.

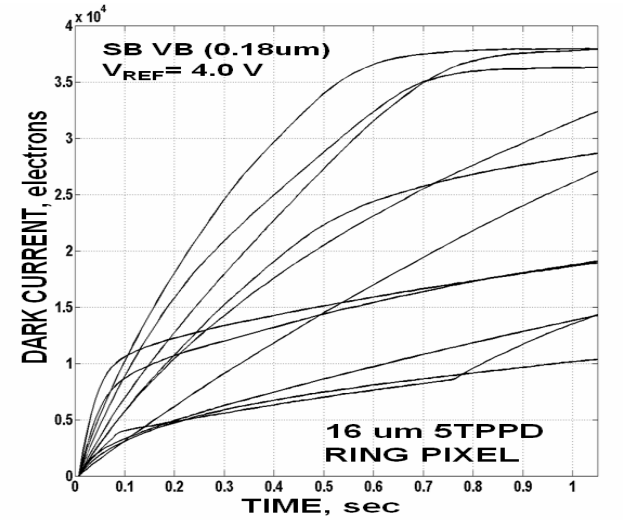

Figure 89. Spikes as a function of integration time.

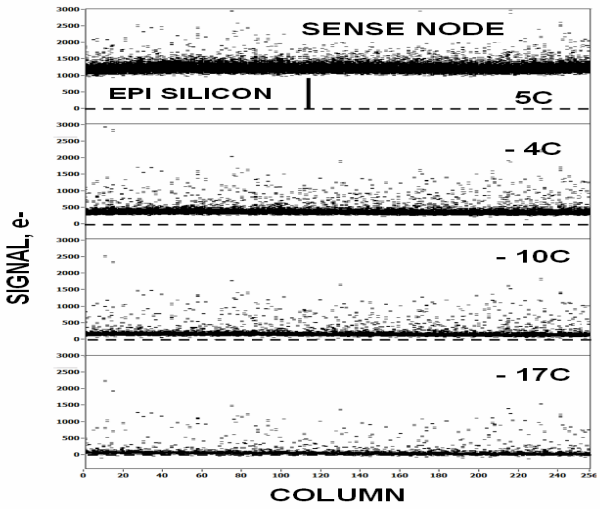

Figure 90. 5TPPD pixel spikes as function of temperature.

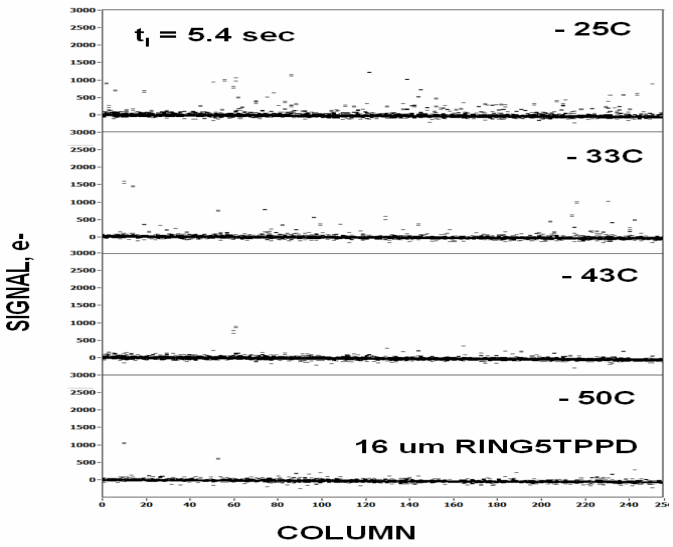

Figure 91. Spikes as function of operating temperature.

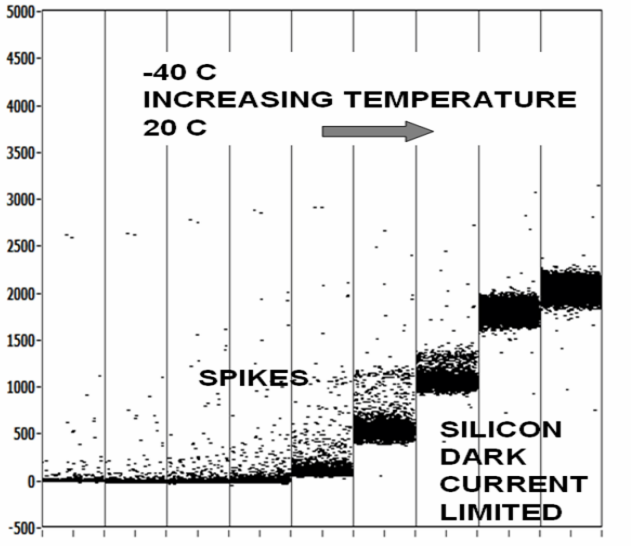

Figure 92. Spikes as function of operating temperature.

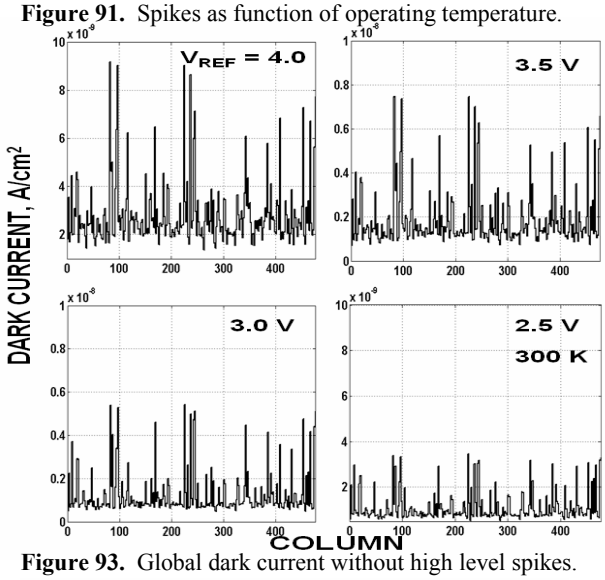

Figure 93. Global dark current without high level spikes.

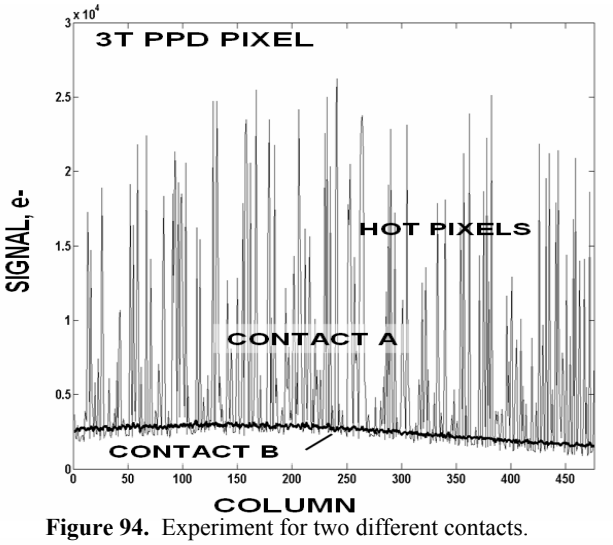

Figure 94. Experiment for two different contacts.

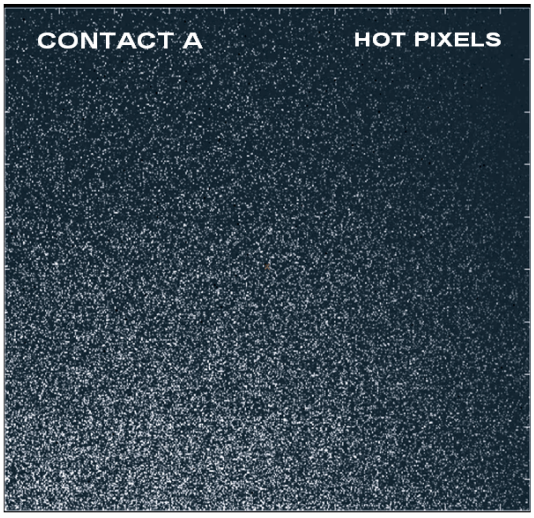

Figure 95. Dark image for Contact A.

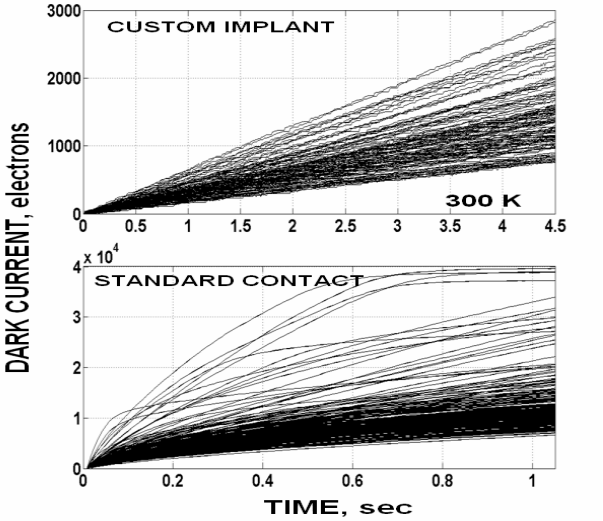

Figure 96. Dark current for custom and standard contacts.

at room temperature (300 K). In comparison, the lower plot shows dark current generated by 3TPPD pixels fabricated with a standard contact (0.18um process). In this case, some pixels generate dark spikes as high as 40,000 e-/sec. Figure 97 shows similar data where dark current is measured in units of nA/cm^2 at 300 K. Note that sense node dark current for the custom process is nearly 40 times lower than the 0.18 um process.

11.2 Dark Current

Figure 98 measures dark current generated within the PPD region of a 8 um 5TPPD BIG MIN I pixel along with a similar designed test pixel that has a PPD region with approximately three times less area. Both pixels are on the same test array and fabricated on 15 um 10,000 ohm-cm epitaxial silicon (refer to Fig. 84). Note that the BIG MIN I pixel generates roughly 3 times more dark current than the test pixel given in electron units and approximately the same rate when expressed in nA/cm^2. Also, past dark current measurements performed for the same pixels fabricated on low resistivity epitaxial (i.e., 3 ohm-cm /7 um epi) produced considerably lower dark current rates of 5 -30 pA/cm^2 depending on how much dark current came from the transfer gate.[1] The high dark current exhibited by high resisitivity silicon is attributed a greater depletion volume compared to 3 ohm-cm material. For 3 ohm-cm material a significant portion of dark carriers generated outside the depletion region recombine.[6] For example, 3 ohm-cm depletes to approximately 1 um whereas 10,000 ohm-cm silicon nearly depletes the 15 um epi layer. Hence, the depletion volume difference between materials is 15^2 or 225 times greater. The BIG MIN I pixel generates more dark current than its test counterpart because its depletion volume is greater (refer to Fig. 58).

Figure 99 compares dark current levels for a 16um 5TPPD RING pixel test imager fabricated on 24 um high-resistivity epitaxial silicon (>10,000 ohm-cm as shown in Fig. 51a). The first graph measures only the sense node dark current whereas the second plot measures sense node and dark current collected by the PPD region of the pixel. The third plot differences the first and second plots to measure PPD dark current alone. Note that nA/cm^2 is approximately 2 times greater than the BIG MIN I pixel because of greater depletion volume. Also the negative spikes observed in the differenced plot are artifacts related to the nonlinearity of the spikes (i.e., the spikes contained in the first plot are higher amplitude than the second plot because the electric fields are greater).

12. RADIATION DAMAGE DATA

This short section presents experimental data for a Sandbox V 256 x 256 x 16um 5TPPD RING Minimal Array irradiated with 100 krd of high-energy 2 MeV electrons. Figure 100 shows RTN baseline and irradiated responses for a row of pixels taken from the array. Figure 101 shows a RTN image for the same row of pixels. As can be seen no new random telegraph signal (RTS) sites are generated after exposure. This curious result has been observed before when irradiating CMOS pixels with Co-60 gamma rays at much higher radiation levels (Ref. 4, Fig. 68). Buried channel results in Figs. 17 and 18 demonstrate that RTN is generated under the gate of the MOSFET presumably by interface states. However, ionizing radiation should in fact be generating new interface states since flat band voltage shift and surface dark current increase are observed. Why significantly more new RTN sites are not induced after radiation remains to be a mystery. Figure 102 shows the relationship between V_{REF} and reset clock level in achieving the hard reset condition before and after irradiation. Note that there is a slight flat band shift of 0.05 V in reset clock drive caused by positive charge build-up under the reset gate. Figure 103 presents a Fe-55 x-ray response after irradiation showing no CTE performance degradation. Figure 104 provides a low-light level CTE square-wave response as a function of TG clock drive. Note that slightly less TG drive is required because of positive charge build up under the gate. Figure 105 shows the dark current increase before and after irradiation for the sense node and PPD region, an expected result. Lastly, Fig. 106 presents an image after irradiation to show that the imager as a whole suffered no dire consequences. Future radiation tests will increase irradiation levels up to 1 Mrd for 2 MeV electrons and 63 MeV protons using the same 256 x 256 x 16 um 5TPPD pixel array.

CMOS radiation hardness results shown in Figs. 100-106 are impressive when compared to a CCD also irradiated with high energy electrons. For example, Fig. 107 presents Fe-55 responses for a 512(H) x 1024(V) frame transfer CCD before and after irradiation to only 3 krds of 10 MeV electrons. Vertical CTE degradation falls from 0.99999 to 0.99959 as a result of bulk silicon damage.[6] Although silicon lattice damage is probably taking place for both CMOS and CCD, CTE performance for the CMOS Minimal Array is maintained since only a single clock pulse is required to transfer charge as opposed to 4 x 1024 transfers for the CCD. In that the gate oxide thickness is significantly thicker for the

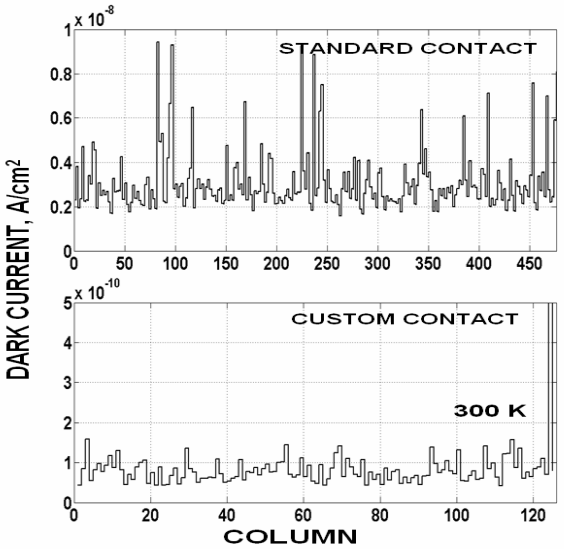

Figure 97. Dark current for custom and standard contacts.

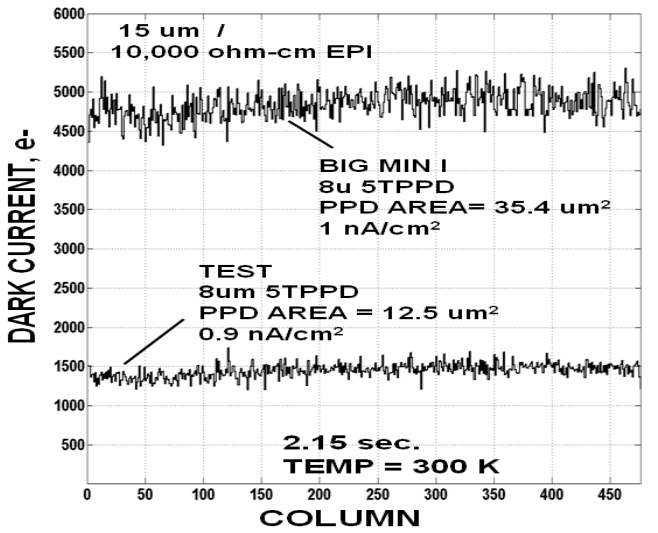

Figure 98. Dark current for two different PPD areas.

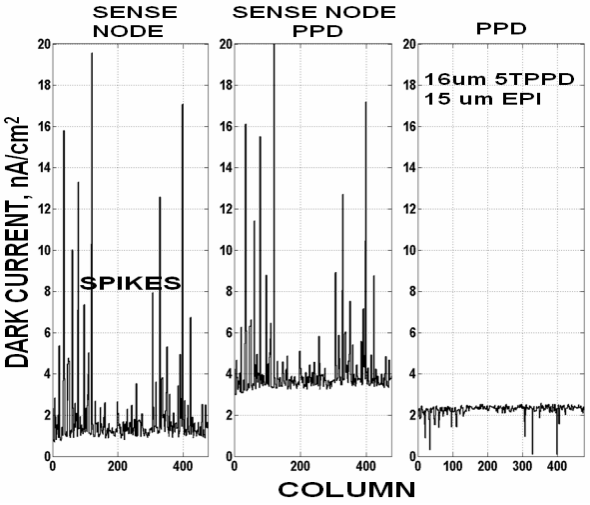

Figure 99. Sense node and PPD dark current.

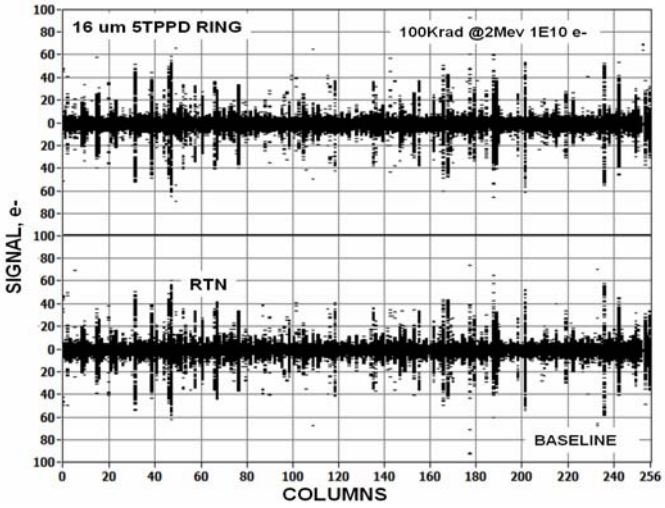

Figure 100. RTN before and after electron irradiation.

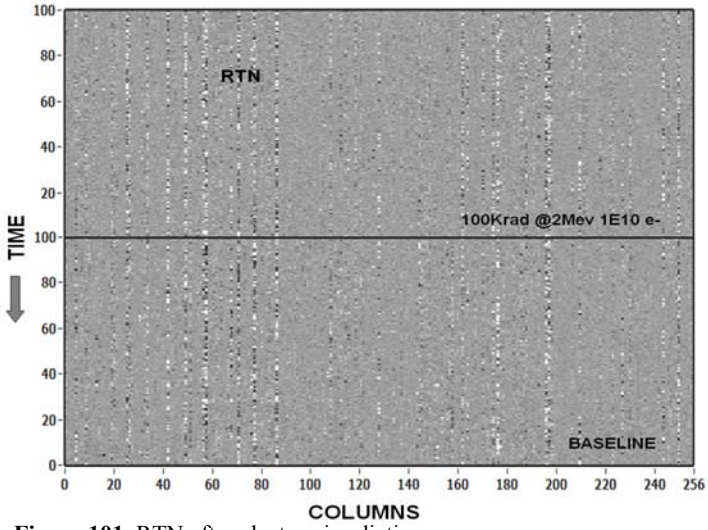

Figure 101. RTN after electron irradiation.

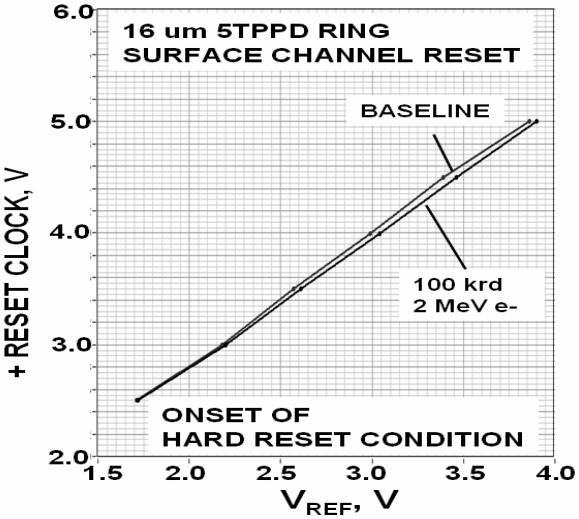

Figure 102. Flat-band shift after 100 krd electron irradiation.

CCD imager more ionization damage occurs. This in turn results in a much greater flat band shift compared to the CMOS pixels. For example, Fig. 108 plots dark signal before and after irradiation to 11.4 krd of 10 MeV e-. Note the irradiated sensor requires approximately 1.2 V more drive to reach the inverted conditions due to positive charge build up under the CCD phases.

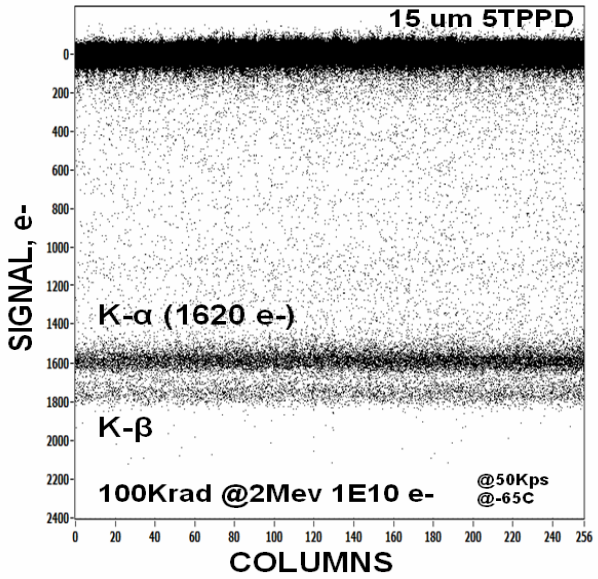

Figure 103. Fe-55 CTE response after electron irradiation.

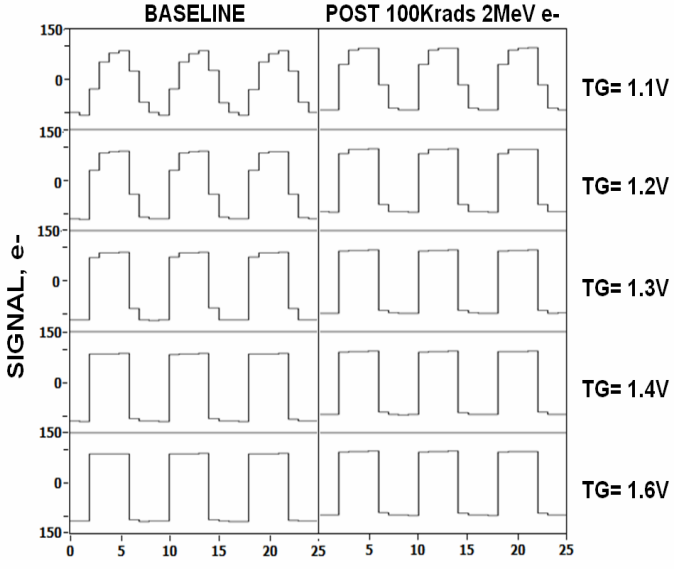

Figure 104. Square-wave CTE response after electron irradiation.

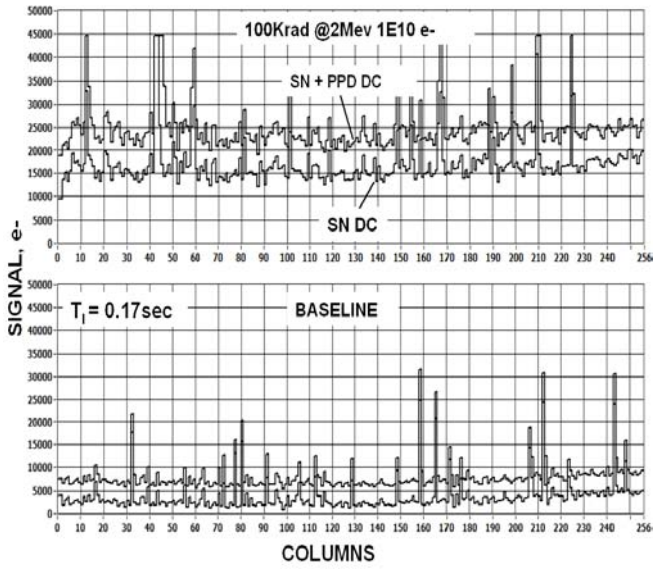

Figure 105. Dark current after electron irradiation.

Figure 106. 5TPPD RING image after 100 krd electron irradiation.

13. FUTURE WORK

The data presented above is derived from a fraction of the new pixels designed on Sandbox V. Therefore, characterization tests will continue for this lot run for years to come. Imagers for Sandbox VC and VI shown in Figs. 109 and 110 currently in fabrication will also require rigorous testing soon. Sandbox VC is primarily intended for buried channel CMOSCCD development whereas Sandbox VI is intended to develop sub-electron signal processing circuitry. Looking ahead, new Sandbox runs involving stitched imager designs is currently a major thrust (e.g., SB VIII discussed above).

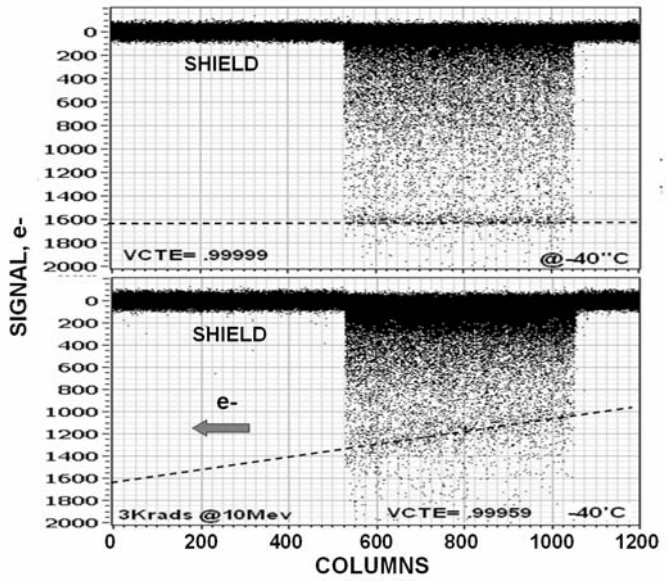

Figure 107. CCD CTE after electron irradiation.

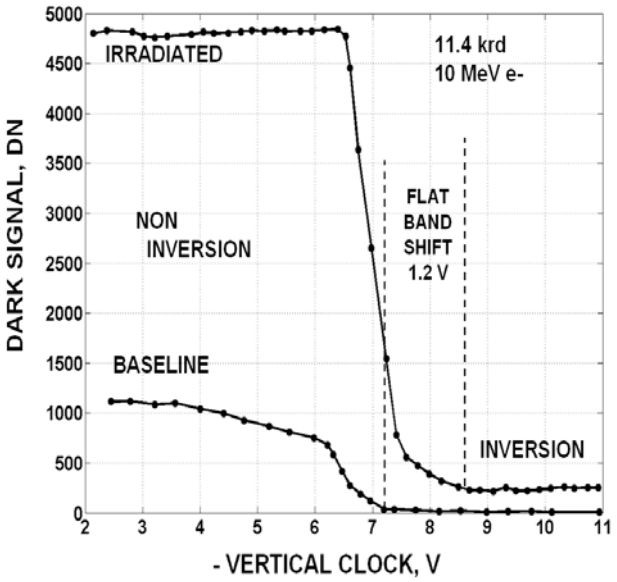

Figure 108. CCD flat band shift after electron irradiation

In parallel with Sandbox imager activities, support and flight electronic development to run and control CMOS imagers above is on going. For example, the 'Minimal Evaluation Test Set (METS)' shown in Figs. 111 and 112 assist interested customers to evaluate imagers in their laboratories. METS specifically runs small Minimal Arrays by providing a simple timing generator, bias voltages, pre-amp, aCDS/dCDS signal chain, 16-bit ADC and digital interface to a 1422 National Instruments frame grabber. Also manual X-Y address switches allow the user to interrogate a single pixel or a specific row of pixels. Full frame readout is possible by addressing and processing a pixel at a time allowing for room temperature operation with sub electron noise performance (refer to Section 5 above for readout details). Progressive scan readout is also provided using the Minimal Array's on-chip signal processing circuitry. METS circuitry is based on a test system that generated data for this and past papers.

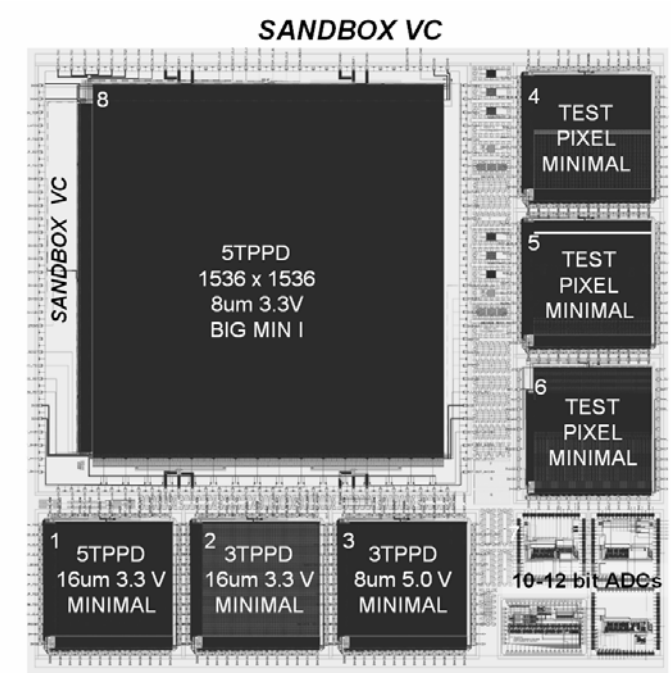

Figure 109. Sandbox VC.

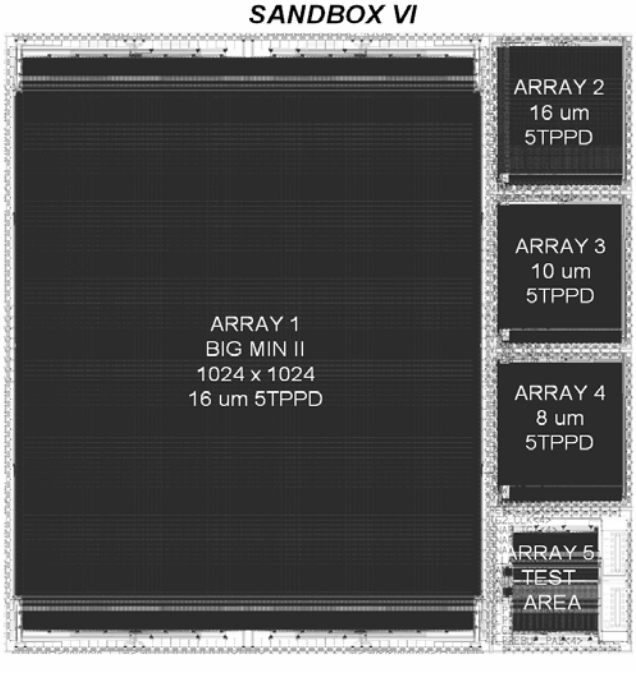

Figure 110. Sandbox VI.

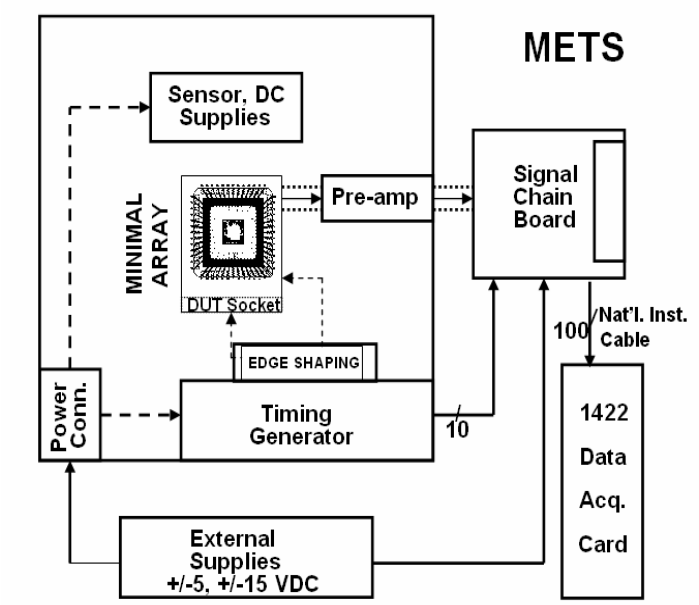

Figure 109. METS block diagram.

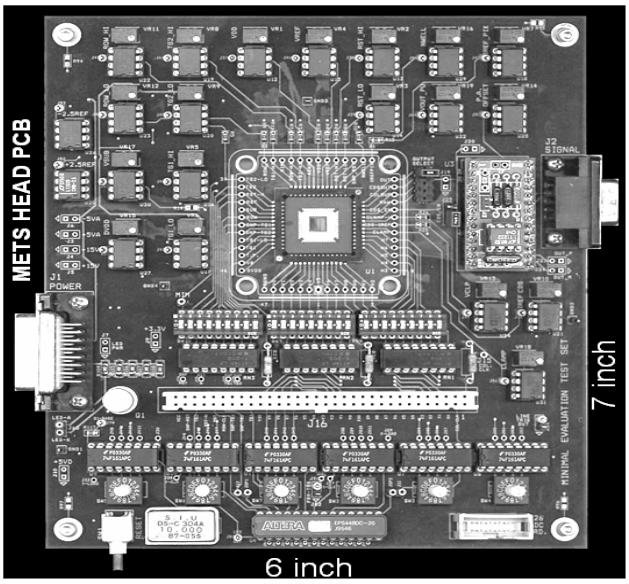

Figure 110. METS head board with Minimal Array installed.

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