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Modifications of the phasemeter firmware since delivery of “as built” documentation

Doc. No.: VLT-TRE-ESO-15734-4535

Issue: 2

Date: 30.11.2012

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CHANGE RECORD

ISSUE	DATE	SECTION/PARA. AFFECTED	REASON/INITIATION DOCUMENTS/REMARKS
1	30/11/2012	All	Creation

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1 Scope

This document describes the modifications applied to the digital phasemeter firmware since the “as-built” documentation was delivered by IMT Neuchatel in 2005.

2 Reference documents

[1] As built Phase Meter configuration for the PRIMA Metrology System, VLT-TRE-IMT-15734-3726, 20.7.2005, O. Scherler, Y. Salvadé, M. Groccia and R. Dändliker

3 Introduction

The phasemeter is a component of the PRIMA metrology which measures the phase between 2 electrical signals. The last stage of the signal processing is a digital phasemeter implemented on a board with programmable logic devices. Since the phasemeter has been delivered to ESO by IMT Neuchatel in 2005 several bugs have been discovered. These bugs have been corrected with the help of the phasemeter provider. This document describes the bugs and the corrections applied to the firmware.

The digital phasemeter is composed of 5 devices implementing 5 tasks (see [1]). The devices are programmed using the software Quartus II. Each of these devices (tasks) is programmed (implemented) via one “program file” (.pof). The five program files are accessed through a global project file (.qpf, which contains also the source files, .bdf). The description of each bug presents the symptom, the concerned source and program files and the modifications. An explanation of the problem is also given.

The procedure used to (re)program the phasemeter board is given at the end of the document in the Appendix (Section 9).

4 First modification of the instantaneous phasemeter

Problem: the output of the instantaneous phasemeter presents discrete “jumps” of amplitude 1024 bits when the phase value is close to an integer multiple of 1024. The bug has been discovered in March 2006 and corrected in September 2006.

Design file affected by modification: Design1.bdf

Programmer object file affected by modification: Design1.pof

Extensive tests done at He-ARC (St-Imier, Switzerland) on the absolute metrology demonstrator have shown discrete fringe jumps at the output of the instantaneous phasemeter. These jumps, of amplitude 1024 bits (1 fringe), appear when the output of the instantaneous phasemeter is an integer multiple of 1024, i.e when the reference and probe signals are in phase. This problem was expected and the instantaneous phasemeter was designed so as to avoid these jumps by using two reference signals phase shifted by $\pi/2$. In that case, one of the reference signals would always be phase shifted with respect to the probe signal. Despite this trick the phasemeter still produces fringe jumps.

Therefore, a new concept has been implemented (see schematics in [Figure 1](#)). It is simpler and uses only one reference signal. The drawback is that, when the reference and probe signals are in phase, some samples may be lost leading to a less efficient averaging of the data. When the signals are in phase the counter triggered by the rising edge of the reference signal is not stop by the first rising edge of the probe signals as the two edges are almost simultaneous. The counter is stopped at the next rising edge of the probe signal. Since the



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counter output is wrapped after 1024 bits and since the two consecutive measurements at 200 kHz are highly correlated it is equivalent to measuring one sample out of two.

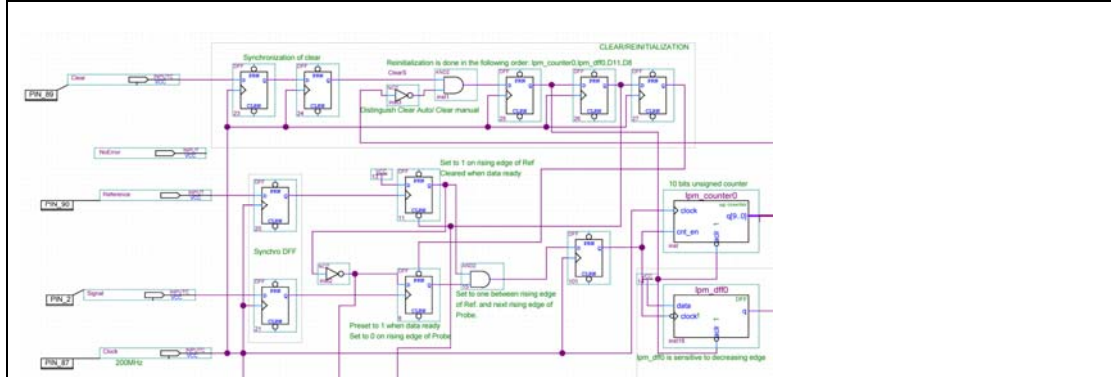


Figure 1: part of the phasemeter PLD that calculates the wrapped phase

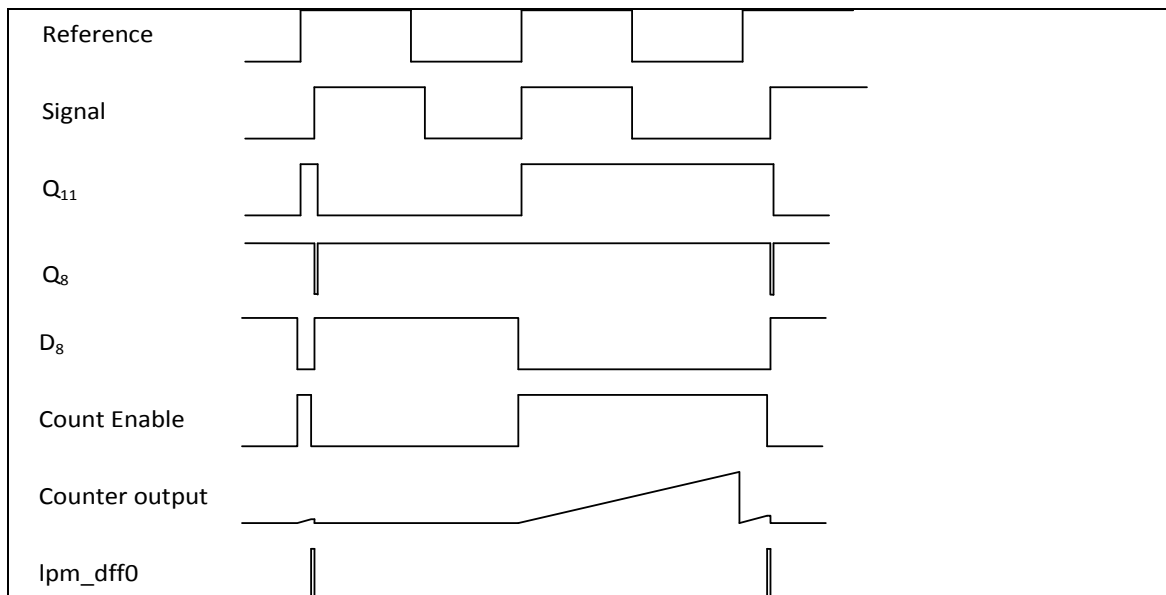


Figure 2: time diagram showing how samples can be lost by the phasemeter when both the reference and probe signals are in phase

This effect is visible in real data provided by the phasemeter as visible in [Figure 3](#). The number of samples can be reduced to half of the number expected for a given sampling frequency.



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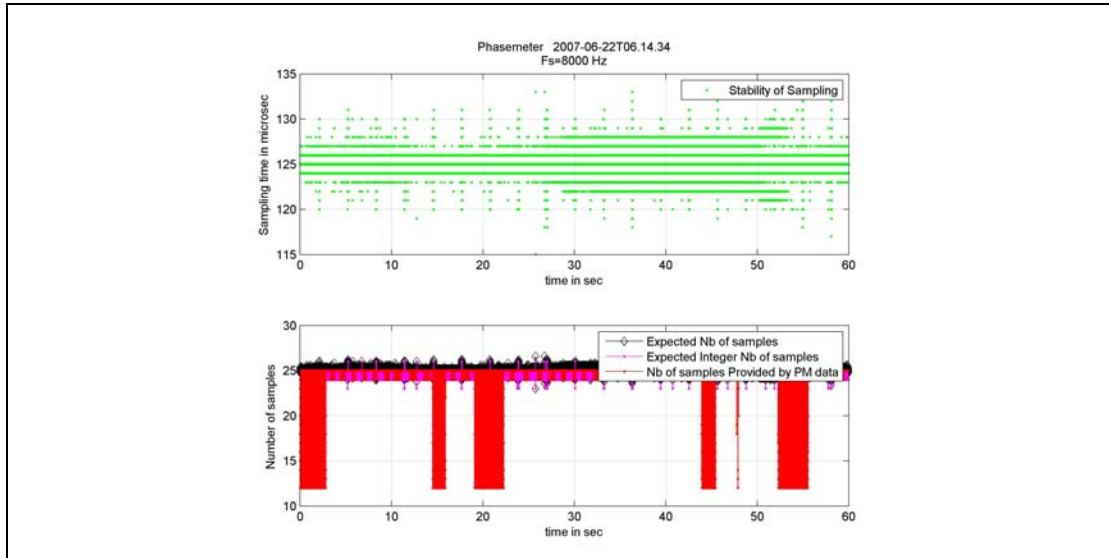


Figure 3: example of a measurement file in which samples have been lost by the phasemeter. The number of samples can drop to half the theoretical value expected from the sampling frequency.

5 Modification of the addresser

Problem: at high sampling frequency the bit of the reset status (indicating a reset has been done) does not change value. Bug discovered and corrected in November 2006.

Design file affected by modification: addresser-slow-strobe-05-01-19.bdf

Programmer object file affected by modification: addresser-slow-strobe-05-01-19.pof

The bit indicating that a reset has been done during the last integration time is generated at the level of the addresser. This part of the firmware creates the signals used to load the data and send them to the LCU.

Quartus II simulations have shown that the problem appears when a trigger occurs just after the reset has been released (see [Figure 4](#)). In that case the rising edge of the clear signal acts as a trigger and starts the sequence which loads the data and starts the strobe signal. It also clears the reset status bit. If the real trigger arrives just after the end of the clear it overwrites the buffer and the reset status bit sent by the phasemeter is 0 instead of 1. The problem was due to the reset of the count enable of the counter S[8..0] caused by the clear of the flip-flop 5 and 37. It has been suppressed.



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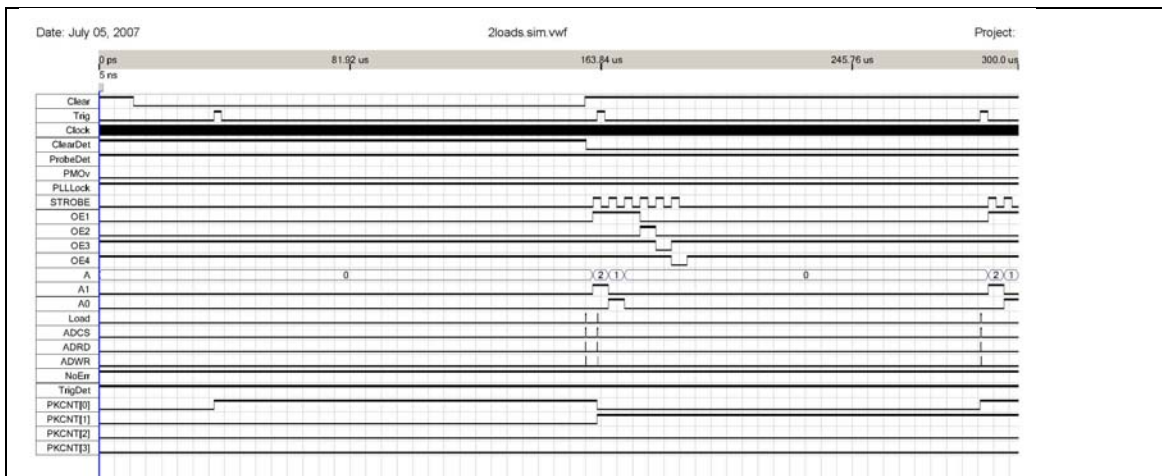


Figure 4: example of Quartus II simulation showing that the trigger generates a second load signal which overwrites the data in the buffers

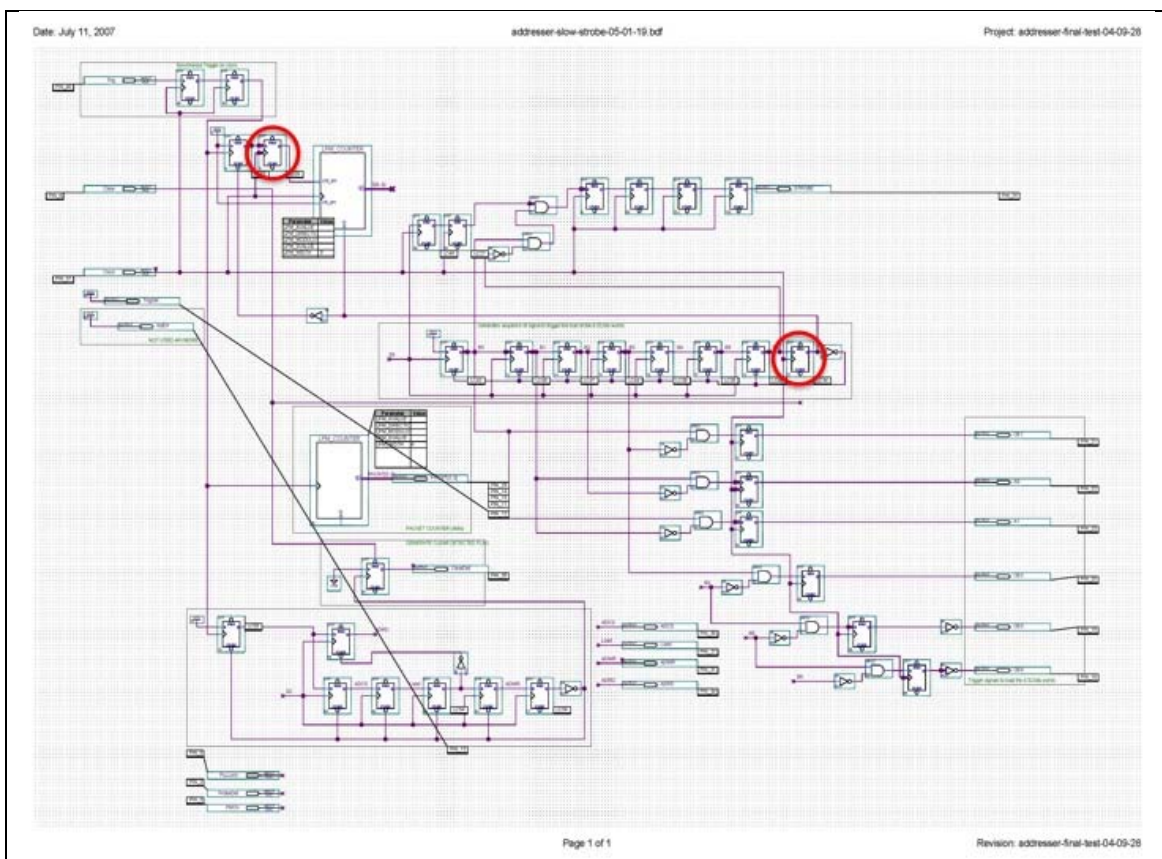


Figure 5: new design file of the addresser; in red are highlighted the flip-flop for which the clear signal has been removed.

6 Modification of the phase adder

Problem: for OPD close to 0, spikes appear in the OPD data. These spikes have amplitudes much larger than the maximum size of the instantaneous phase counter and are created at the level of the phase adder.

Design file affected by modification: phaseadder200-03-05-07.bdf

Programmer object file affected by modification: phaseadder200-03-05-07.pof

The instantaneous phasemeter produces after each measurement of the phase (i.e at 200 kHz) a signal “ready” which triggers the phase adder and increments the sample counter. On the rising edge of the signal “ready”, the phase adder sums the instantaneous phase with the sum of the phases of the previous samples. Its output is propagated when the phasemeter is triggered. The phase adder uses combinatory logic and the propagation of the results is not instantaneous. Consequently, if a trigger and a signal “ready” arrive simultaneously, the value of the phase adder loaded in the buffer may not have had the time to stabilize at the right value. In order to let the phase adder output stabilize at the right value, the signal ready must be disabled if it happens just after a trigger. This has been implemented by replacing the count enable signal of element 10 and 49 by a unique one on the flip flop 155 (see Figure 6). One clock signal after the trigger has arrived the signal ready is disabled, three clock signals later the phase sum is loaded in the buffer and after five more clock signals the signal ready is enabled again.

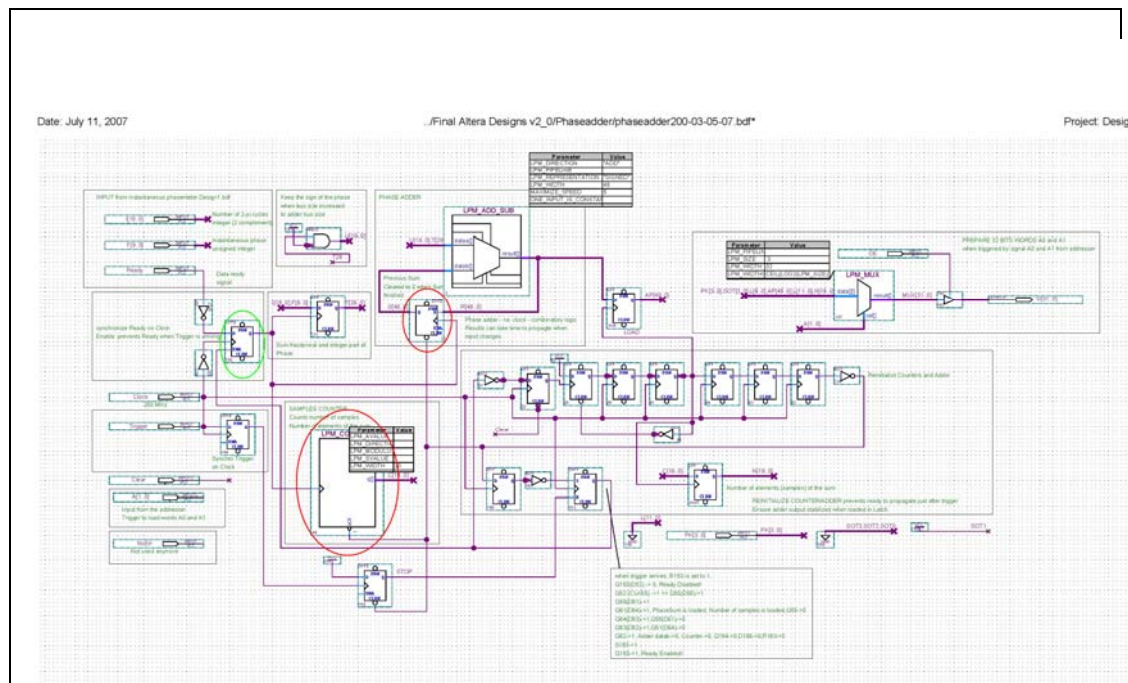


Figure 6: modifications applied to the phase adder; in red are highlighted the elements for which the enabled signal was suppressed; in green is highlighted the element that prevents the signal ready after a trigger.

7 2nd modification of the phasemeter



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Problem: the instantaneous phasemeter gets stuck and stops delivering data. Bug discovered and corrected in October 2007. ESO phasemeters have been upgraded in January 2008.

Design file affected by modification: Design1.bdf

Programmer object file affected by modification: Design1.pof

A test campaign on the absolute metrology system, carried out in October 2007, has revealed a strange behavior of one digital phasemeter board (board belonging to He-ARC, part of the first series of build phasemeters). The instantaneous phasemeter kept getting stuck without reason. The instantaneous phasemeter architecture has been upgraded a second time to solve this problem. Although this failure has not been detected on any ESO board (spare 1,2 and 4), they have all been upgraded. The new instantaneous phasemeter is described in **Error! Reference source not found..**

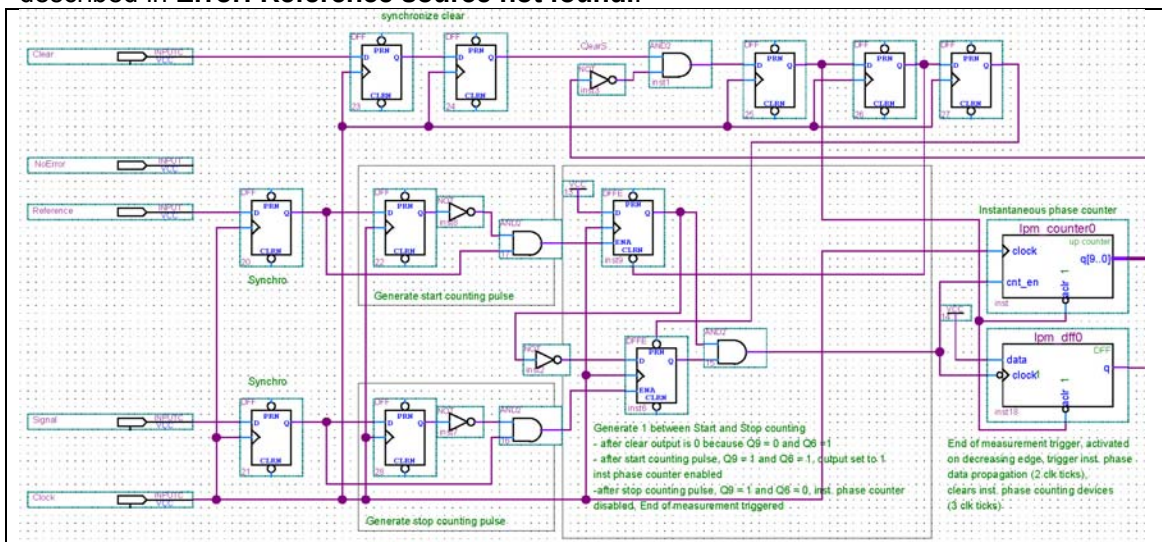


Figure 7: second upgrade of the instantaneous phasemeter. It solves a problem that appeared only on He-ARC board. However, ESO boards have been upgraded as well.

8 3rd modification of the phasemeter

Problem: reduce frequency of the fringe counter wrapping and enable the FC overflow flag for unwrapping when the metrology sampling frequency is 4 kHz (although unwrapping should not be needed as a wrapping will occur only after 1 hour and 20 minutes after a reset of the phasemeter which is much than the expected observation block length).

Firmware version: v2.1

Pmacq version: v0.79.1.4 (for the lcu to interpret the fringe counter as a 32 bits signed).

8.1 introduction

PRIMET measures a differential OPD between two interferometers. The architecture of PRIMET is such that it computes the differential OPD directly from 2 heterodyne signals obtained with two slightly difference optical frequencies separated by $\Delta\nu = 78$ MHz.

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The phase difference of the two heterodyne signals is given by:

$$\Delta\Phi = \Phi_1 - \Phi_2 = \frac{4\pi\nu}{c}\Delta OPD - \frac{4\pi\Delta\nu}{c}OPD_2$$

where c is the speed of light, ΔOPD the differential OPD, ν the optical frequency of the first interferometer and OPD_2 the OPD in the second interferometer. Therefore OPD_2 must be measured in order to derive ΔOPD . Due to the small value of the corrective term it is enough to know the number of fringes in the second interferometer to estimate OPD_2 .

$$OPD_2 = nbrFringes \times \lambda_2$$

where $nbrFringes$ is the number of fringes and λ_2 the wavelength used in the second interferometer.

The fringe counting is done in a dedicated chip of the digital phasemeter board.

8.2 Design before modification and some numbers

In the present design the fringes are counted as follows:

- One counter counts the number of rising edges of the 450 kHz reference signal of the interferometer; this counter has 24 bits;
- One counter counts the number of rising edges of the 450 kHz probe signal of the interferometer; this counter has 24 bits;
- The output of the probe counter is subtracted to the output of the reference counter and the result is passed as a number of fringes coded over 25 bits (signed) to the buffer for transfer to the LCU.

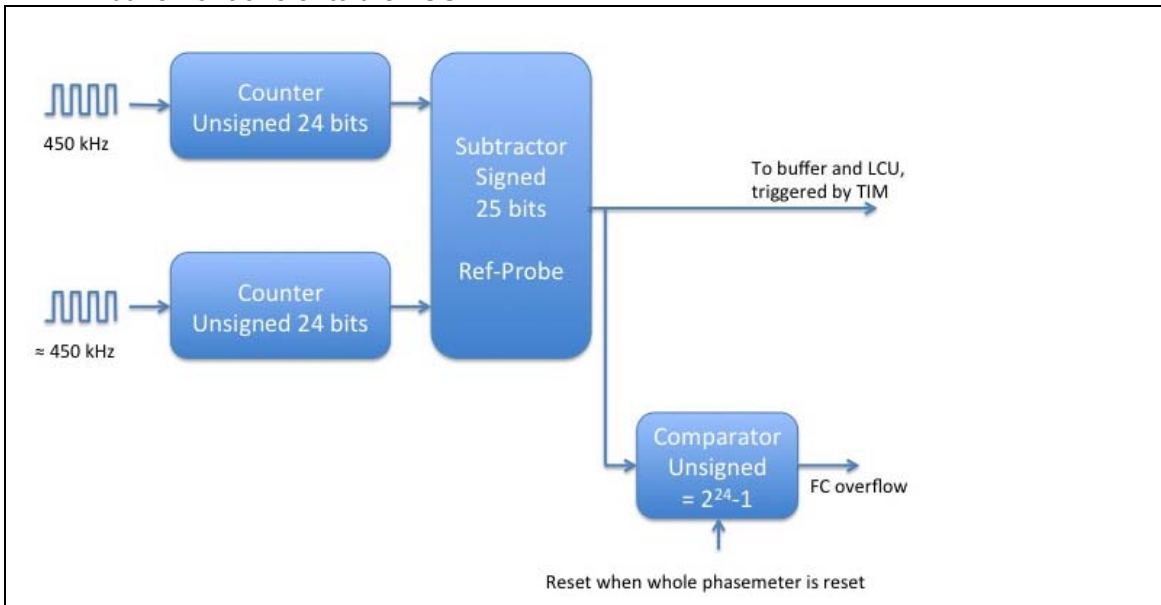


Figure 8: schematic of the present implementation, the flag FC overflow is set once and for all (until a phasemeter reset) when the fringe number difference is exactly $2^{24}-1$.

As a consequence, the output value which contains the number of fringes can jump:



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- When the reference counter wraps, which happens every $224/450\text{e3} = 37.3\text{s}$; the amplitude of the jump is 2^{24} fringes, i.e $1.9\text{ }\mu\text{m}$.
- When the probe counters wraps, which happens approximately every $2^{24}/450\text{e3} = 37.3\text{ s}$ depending on the DL speed; the amplitude of the jump is 2^{24} fringes, i.e $1.9\text{ }\mu\text{m}$.
- When the output of the subtractor wraps which happens only in two cases, the first counter is full and the second empty and conversely the first is empty and the second is full, the amplitude of the jump is 2^{25} fringes, i.e $3.8\text{ }\mu\text{m}$.

The first two kinds of jump are common and can happen very close in time if the speed between the two delay lines is slow and as their signs are opposites it can give the impression of a spike (see mail from J. Sahlmann “PRIMET 1.9 micron double-step”).

The flag appears only for the third type of wrapping and stays enabled until the phasemeter is reset.

8.3 New design

Studying the firmware and lcu software of the phasemeter we noticed that it was in fact possible to not only implement larger counters on the board but also to send larger values to the lcu. The fringe number was sent as a 25 bits signed number in a 32 bits word whose first 7 bits were unused. Consequently, the new firmware implements two 31 bits counters instead of the 24 bits counters and one 32 bits subtractor instead of the 25 bits subtractor. The number of fringes sent to the lcu is coded as a signed 32 bits. The lcu software was corrected accordingly by R. Frahm (pmaq v0.79.1.4).

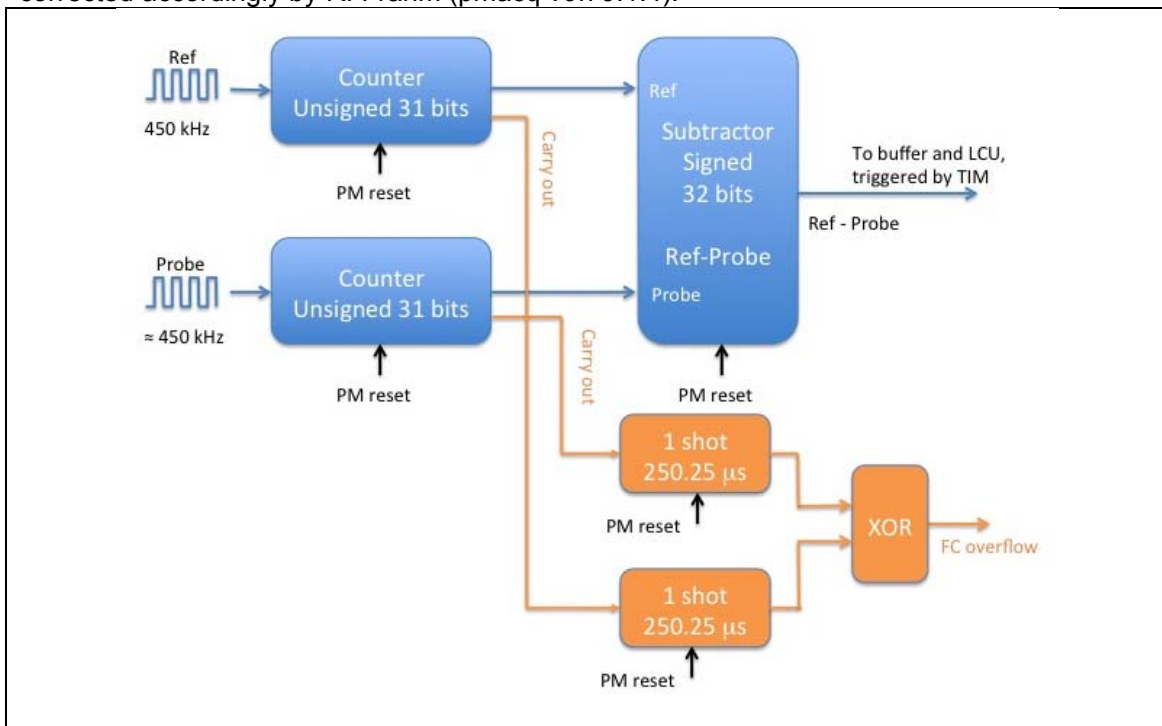


Figure 9: schematic of the new design of the fringe counter in the firmware v2.1.

As a consequence, the output value which contains the number of fringes can jump:



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- When the reference counter wraps, which happens every $2^{31}/450\text{e3} = 1.37$ hours; the amplitude of the jump is 2^{31} fringes, i.e 485.12 μm .
- When the probe counters wraps, which happens approximately every $2^{31}/450\text{e3} = 1.37$ hours depending on the DL speed; the amplitude of the jump is 2^{31} fringes, i.e 485.12 μm .
- When the output of the subtractor wraps which happens only in two cases, the first counter is full and the second empty and conversely the first is empty and the second is full, the amplitude of the jump is 2^{32} fringes, i.e 920.24 μm .

The overflow of one counter, through its carry-out bit, triggers a pulse of 250.25 μs to make sure that the flag level is high when the next trigger sent by the lcu arrives. Of course this value works only for a sampling rate of 4 kHz. As the chip implementing the fringe counters is not connected to the trigger, it is not possible to implement a mechanism independent of the sampling frequency.

An XOR is used to combine the flag of each counter to prevent from sending the flag to the lcu when the two counters wrap between the same 2 triggers. Indeed, in that case the two wrappings compensate for each other and the FC value sent to the lcu does not present any jump with respect to the previous value.

9 Conclusion

The last version of the firmware is V.2.1 associated with pmaq v0.79.1.4.

10 Appendix: how to (re)load the digital phasemeter firmware

Prerequisites:

- Quartus II software is installed on a PC with an available parallel communication port (Quartus II can be downloaded freely at <http://www.altera.com/products/software/products/quartus2/qts-index.html>, the licence file can be downloaded for free on the same website);
- ByteBlaster II Parallel Port Download Cable (<http://www.buyaltera.com/scripts/partsearch.dll/partdetail?site=ALTERA;lang=EN;part=544-1289-ND>);
- Voltage generator (5V);
- “Final AlteraDesign 30.10.07.zip” containing the firmware project.

Procedure:

- (1) Start **Quartus II** and load the firmware project (open “**Design1.qpf**” file);
 - (2) Check with a voltmeter that the generator is set to provide **5V**;
 - (3) Connect the Phasemeter to the voltage generator as follows (see also Phasemeter as-built report [1] and **Error! Reference source not found.**):
- Ground to connector J1 pin C9;

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- 5V to connector J1 pin A32;
- (4) Connect the PC to the phasemeter digital board using the “ByteBlaster II Parallel Port Download Cable”;
- (5) Power up the voltage generator to provide **5V** to the digital phasemeter board;
- (6) In Quartus II launch the **Programmer** (Tools->Programmer);
- (7) Set the hardware set-up to: **ByteBlaster [LPT1]**;
- (8) In the table the 5 program files should appear as in **Error! Reference source not found.**;
- (9) Verify that the boxes “**Program/Configure**” and “**Verify**” are checked on the line of the program file you want to program/reprogram;
- (10) Verify that the other options are **NOT CHECKED**;
- (11) The configuration is ready, click on **START** to begin the program procedure which lasts from a few seconds to a few minutes depending the on how many files are being programmed;
- (12) Switch off the voltage generator;
- (13) Disconnect the board.

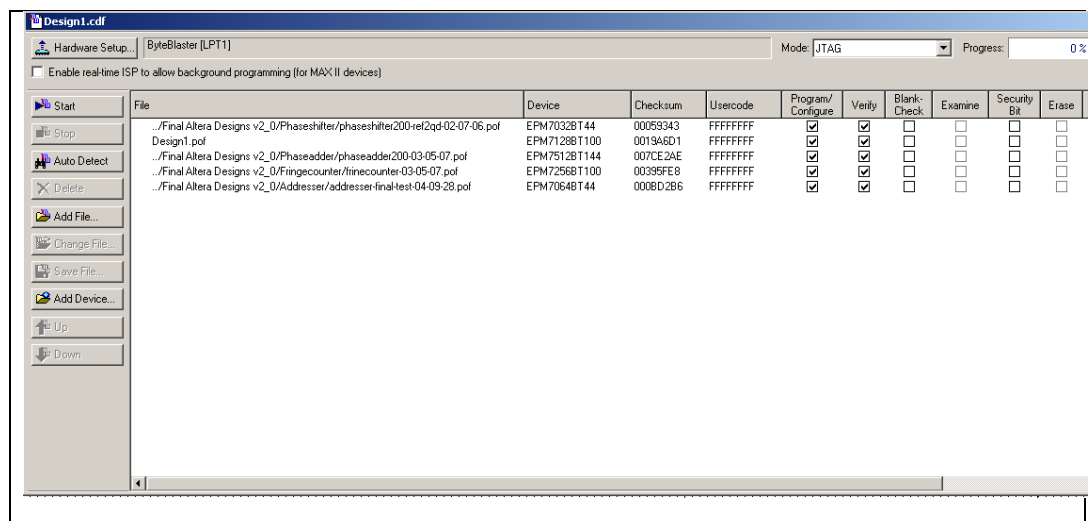


Figure 10: configuration of the Quartus II programmer to program the 5 devices of the digital phasemeter board. The board is programmed through the PC parallel port using ByteBlaster and the corresponding cable.

