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VERY LARGE TELESCOPE

Specifications for high sensitive 4-quadrant detectors for the PRIMA Metrology System

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CHANGE RECORD

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1 INTRODUCTION

This document presents the technical specifications for high sensitive infrared 4-quadrant detectors for the PRIMA laser metrology system [AD 1].
The objective is to measure sub-microns displacement of 1mm diameter laser beam at a wavelength of 1319nm and for low power (down to <100nW).

Reference Documents

Ref	Document Number	Issue	Date	Title
AD 1	VLT-TRE-ESO-15730-3000	1	12/1/04	Design Description of the PRIMA Metrology System.
AD3	VLT-SPE-ESO-10000-0015	5	6/3/01	VLT Electronic Design Specifications

List of Abbreviations/Acronyms

LCU: Local Control Unit
PCB: Printed Circuit Board
TBD: To Be Defined
TBC: To Be Confirmed

2 SYSTEM DEFINITION

The 4-quadrant detector system consists of:

- 1x detector head : 1 InGaAs 4-quadrant chip, low noise transimpedance amplifier, gain selection
- 1x30m cable relaying the signals Q1, Q2, Q3, Q4 to the acquisition module and providing power to the detector head
- 1 acquisition module (per 4-quadrant detector) located in a 3HE-8TE module. This module filters the quadrant signals and provides power to the detector head.
- 1x 19 inches rack which hosts up to 8 acquisition modules and 1 power supply

The acquisition module provides 4 analog signals which can be read by a 16 bits Analog input board (VMIVME3123) located inside a LCU: Q1,Q2,Q3,Q4: 0-10V

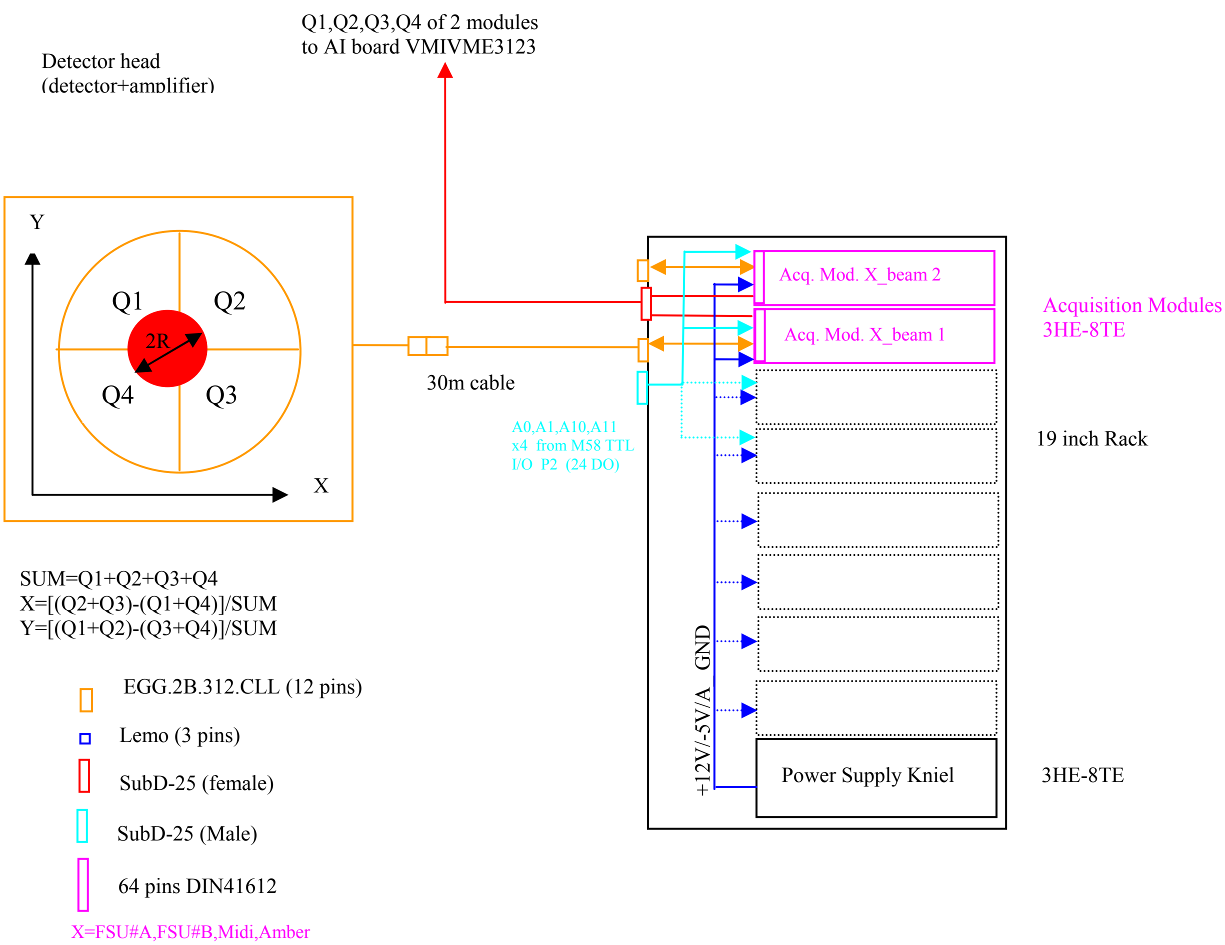


Figure 1: Configuration of the 4-quadrants detector

3 SYSTEM PERFORMANCE

Range: +/- R where R is the laser spot radius (baseline R=0.5mm)
Optical wavelength : 1319 nm
Optical saturation levels: identical to the prototype values, i.e 13 µW, 1.3 µW, 130nW according to the selected gain.
Bandwidth: 250 Hz
Thermal dissipation of the detector head: < 2.5 W (goal <1.25 W)
Noise level:

Dark Peak-to-Peak variation of the Q's voltages over the bandwidth [2.7e-4;250Hz]: ≤ 10mV (including the drift of the offset compensation over 1 hour)

4 HARDWARE REQUIREMENTS

4-quadrant detector head:

3 mm diameter, InGaAs 4-quadrant detectors: EOSystems (IGA-030-QD) WITHOUT window
Low noise operational amplifier: OPA2380
Transimpedance amplifier:
Gain: 10^6 (resistor: 1 MOhm , exchangeable)
Bandwidth: 2kHz (capacitance of 80pf or closest value, exchangeable)
Zero compensation using accessible potentiometer (TBC)
Programmable gain: PGA 204

Output connector: Lemo connector
Electrical Test points:
at the output of the transimpedance amplifier of each quadrant
at the output of the programmable amplifier of each quadrant

Cable between the detector head and the acquisition module:
30m long, low noise shielded cable, mounted with 12 pins lemo connectors

Acquisition Module
3U-8TE module (RS 291-7118) with DIN41612 connector (2 rows 64pins)
Operational amplifier: TBD
SW selectable gain of the PGA204 (1,10,100) using A0, A1, D_gnd digital input
SW selectable gain of the transimpedance amplifier using A10, A11, D_gnd digital input
HW selectable gain of the PGA 204 (1,10,100) using front panel switch (directly soldered to the PCB)
HW selectable gain of the transimpedance amplifier on the detector head
Switch between SW and HW gain defined by front panel switch (PGA204) and by a switch on the detector head (transmpedance amplifiers)
Bandpass filter: 250 Hz (exchangeable resistors and capacitance)
Electrical Test points:
Q1raw, Q2raw, Q3raw, Q4raw delivered by the detector head and measured at the input of the acquisition module (before filtering by the acquisition module)

5 INTERFACE DEFINITION

5.1 Detector head

5.1.1 Mechanical interface

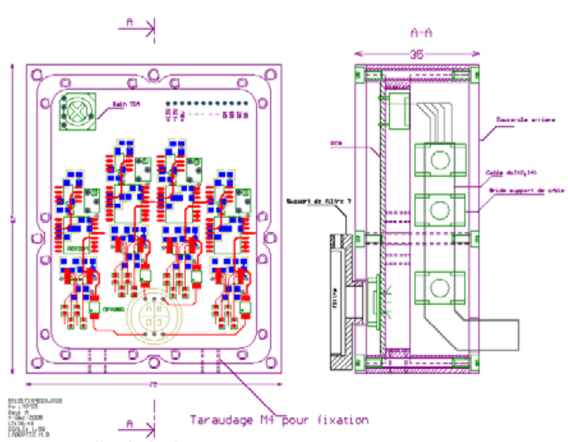
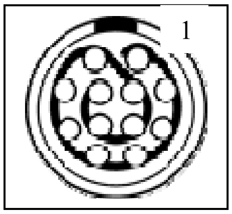
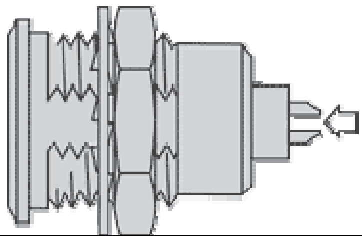


Figure 2: Detector head mechanical configuration

5.1.2 Electrical interface

Lemo connector EGG.2B.312.CLL





Pin of the Lemo EGG.2B.312.CLL	Description
1.	AGND
2.	-12V
3.	+ 12V
4.	n.c
5.	AA0 (for PGA204)
6.	AA1 (for PGA204)
7.	A10 (for transimpedance)
8.	A11 (for transimpedance)
9.	Q4 Raw
10.	Q3 Raw
11.	Q2 Raw
12.	Q1 Raw

5.2 Acquisition module

5.2.1 Mechanical interface

3HE-8TE modules (RS 291-7118) hosting a 100x160mm Europa Card. A DIN41612 connector (2 rows 64pins) shall be mounted on the Europa Card.

2x Front panel switches:

- Definition of the HW gain (A0 and A1 of PGA204)
- Switch between SW and HW gain (switch with locking system)

1xLED on the front panel to indicate if the module is powered.

5.2.2 Electrical interface

The acquisition module of each detector is plugged on the back plane of the 19inches rack using a DIN41612 connector (2 rows 64 pins). The pin plan is given here below:

	Pin Number	Row A	Row C
Signals to the LCU via SubD-25	1.	Q1 [0 +10V]	AGND
	2.	Q2 [0 +10V]	AGND
	3.	Q3 [0 +10V]	AGND
	4.	Q4 [0 +10V]	AGND
Test signals	5.	n.c	n.c
	6.	Test Q1 raw	Test Q2raw
	7.	Test Q3 raw	Test Q4 raw
Signals connected through one Lemo EGG.2B.312.CLL To/From detector head	8.	Q1 raw	Q2 raw
	9.	Q3 raw	Q4 raw
	10.	n.c	n.c
	11.	AA0 (for PGA204)	AA1 (for PGA204)
	12.	A10 (for transimpedance)	A11 (for transimpedance)
	13.	n.c	n.c
	14.	n.c	n.c
	15.	n.c	n.c
	16.	-12V	n.c
	17.	n.c	n.c
	18.	+12V	n.c
	19.	n.c	n.c
	20.	AGND	n.c
	21.	n.c	n.c
Signals from power supply/digital line	22.	A0 [TTL]	A1 [TTL]
	23.	A10 [TTL]	A11 [TTL]
	24.	n.c	n.c
	25.	n.c	n.c
	26.	-12V	-12V
	27.	n.c	n.c
	28.	+12V	+12V
	29.	n.c	n.c
	30.	DGND	DGND
	31.	n.c	n.c
	32.	AGND	AGND

SW Gain Selection PGA 204

SW_A0	SW_A1	Gain Selection	Gain Value on PGA204
0	0	Software	G=1 A0=0 A1=0
1	0	Software	G=10 A0=1 A1=0
0	1	Software	G=100 A0=0 A1=1
1	1	Software	G=1000 A0=1 A1=1: **NOT USED**

Note: logical states 1 for V>2 V;

SW Gain Selection Transimpedance

SW_A10	SW_A11	Gain Selection	Gain Value on Transimpedance
0	0	Software	G0=1
1	0	Software	G1 =2.2
0	1	Software	G2= 5.7
1	1	Software	G3=10

Note: logical states 1 for V>2 V;

6 DELIVERABLES

- InGaAs 4 quadrant detector heads and associated acquisition modules
- Detailed PIN plan of the detector head and acquisition module
- Detailed electronic layout of the detector head and the acquisition module

7 ESO FURNISHED EQUIPMENT

7.1 List of equipment

1x19 inch rack.
1xPower supply Kniel CAD 5.4/12.2 (24 W, 5V, +/-12 V); Article number: 173-004-02
8x 3HE-8TE modules (RS 291-7118)
Interface cables inside the rack:

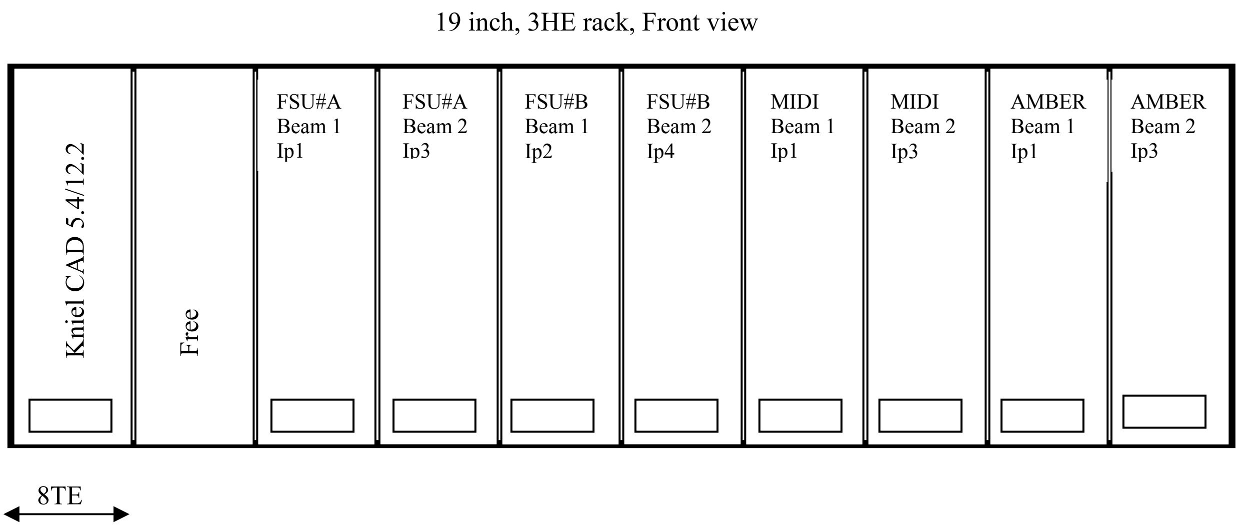
64 pins DIN41612 to 12 pins Lemo EGG.2B.312.CLL (Q1, Q2, Q3, Q4, -5V, +12V,A0, A1,A10,A11,Gnd)
64 pins DIN41612 to subD25 (female) (Q1, Q2, Q3, Q4 of 4 modules, i.e 16 cables)
2 pins Lemo to 64 pins DIN41612   (A0,A1)
Power socket to Kniel CAD 5.4/12.2
Kniel CAD 5.4/12.2 to 64 pins DIN41612 (+12V/-5V/GND)

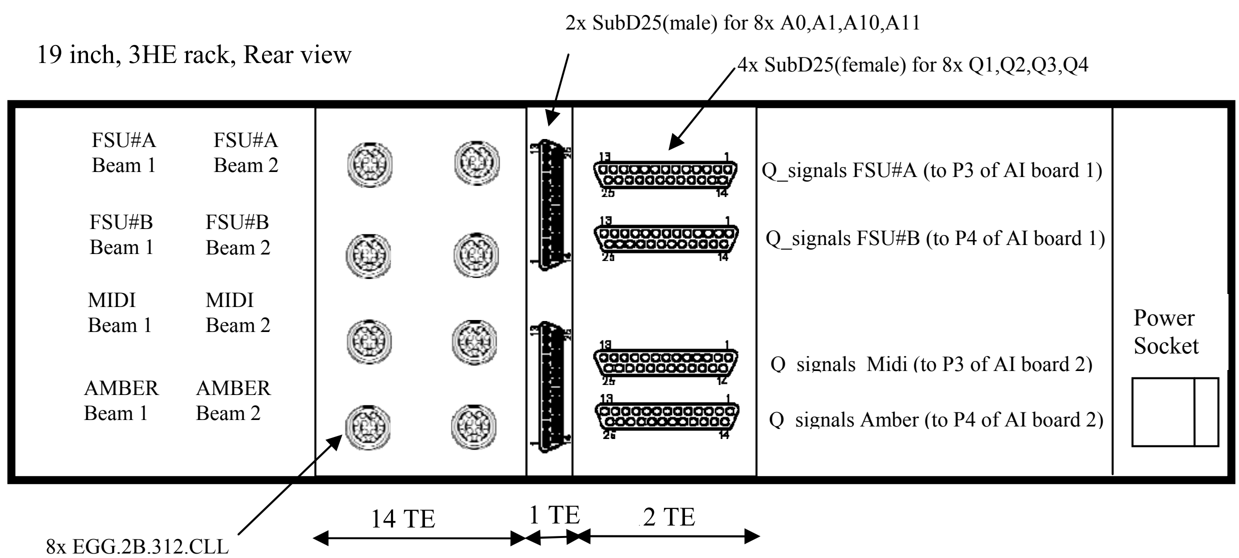
4 Interface cables from the 4 subD25 (female) of the rack to the subD25 (female) of 2 Analog Input boards VMIVME3123

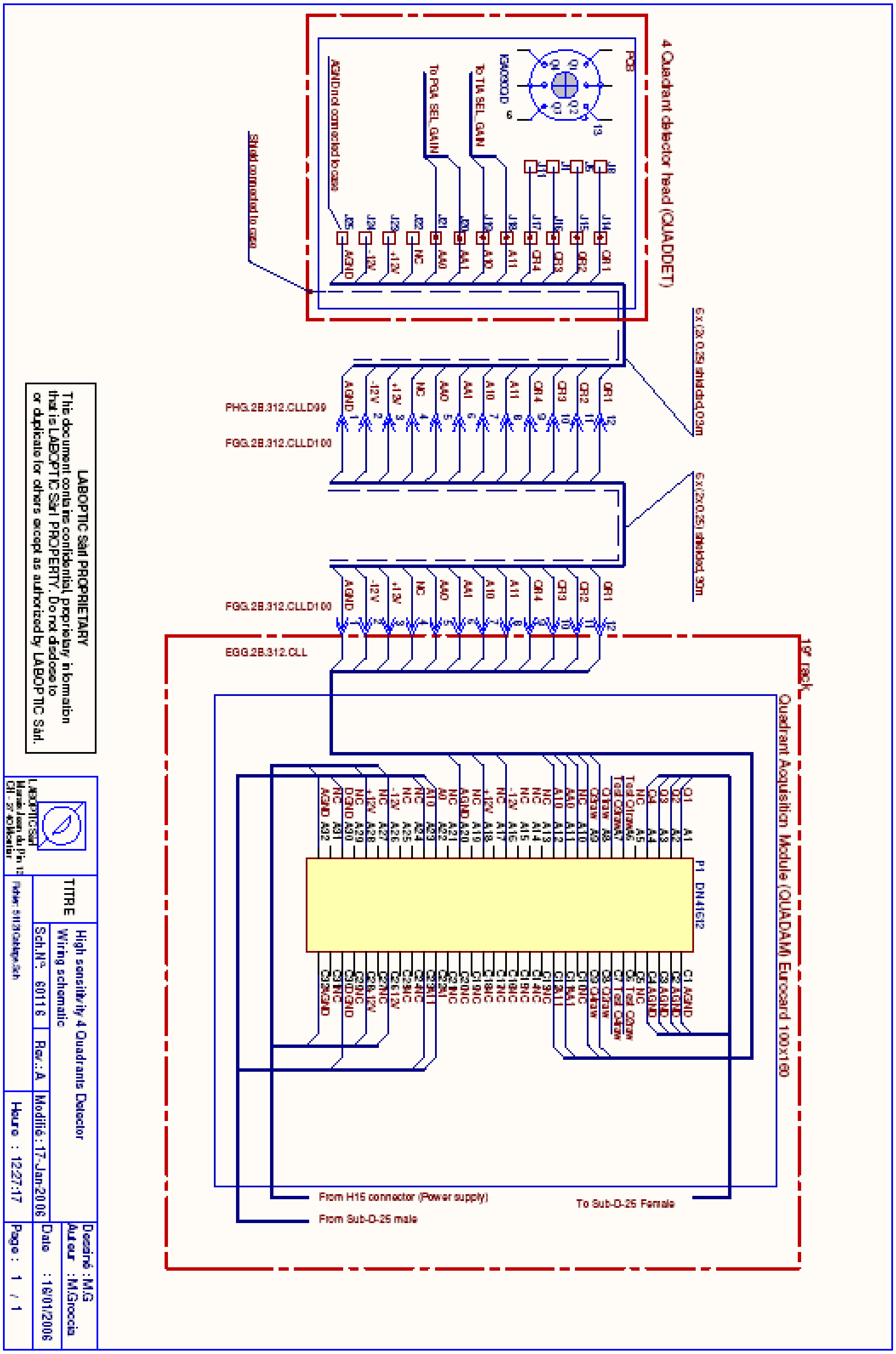
2 Interface cables from the 2 subD25 (male) of the rack to 2 Digital Output M-Modules (M58)

7.2 Pin plan of the 19" rack1

7.2.1 General Layout







4 Quadrant detector head (QUADDET)
19" rack
Quadrant Acquisition Module (QUADAM) Eurocard 100x160
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High sensitivity 4 Quadrants Detector
Wiring schematic
From H15 connector (Power supply)
From Sub-D-25 male
To Sub-D-25 Female

7.2.2 Connection of the Kniel power supply

Reference: Kniel `low-emission-regulator CAD 12.2`
```
power supply:
p/n: 173-001-02
input: 115/230 Vac
output: U1=12Vdc 2,0A; U2=12Vdc 2,0A
dimensions: 8HP/3U
front panel: anodized.
```

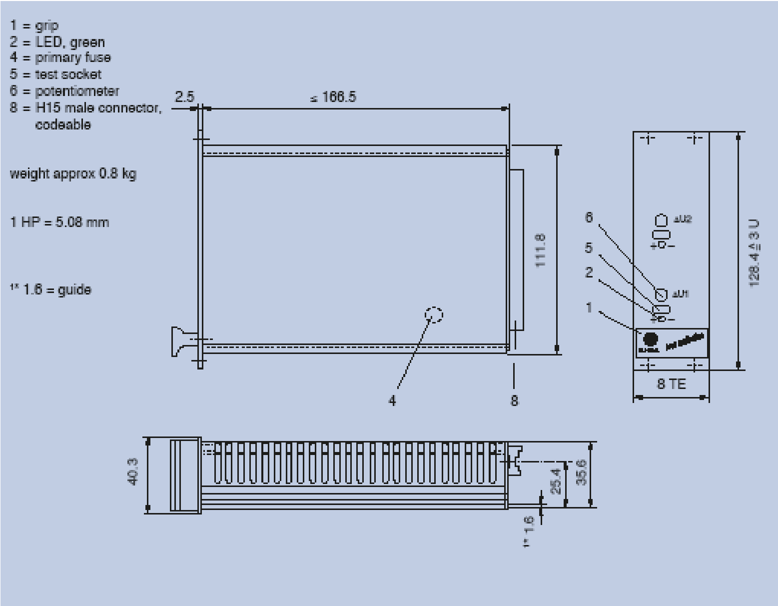
low emission AC/DC-Converters 19"/3 U

Double Outputs

up to 48 W

KNIEL

Dimensions in mm



H15 Connector Pin Assignment

	Pin		Pin
+ Output 1	4	– Sense Lead 2	18
+ Sense Lead 1	6	+ Output 2	20
– Output 1	8	– Output 2	22
– Sense Lead 1	10	Live L1	28
O/I External ON/OFF	12	Neutral N	30
+ Sense Lead 2	16	Earth PE	32 leading

Free pins may not be connected external!

H15 Connector Pin	Description	to be connected to
4	+ Output1 (+12V)	Pin 22 of Power supply H15 (-output 2)->defines Analog GND Bus for all DIN41612
6	+ sense lead 1	n.c
8	-Output1 (ref 12V)	Pin 26 row A & C of DIN41612 -> defines -12V Bus for all DIN41612
10	-sense lead 1	n.c
12	0/1 Ext.ON/OFF	n.c
16	+ sense lead 2	n.c
18	- sense lead 2	n.c
20	+output 2 (+12V)	Pin 28 row A & C of DIN41612 -> defines +12V for all DIN41612
22	-Output 2 (Ref 12V)	Pin 4 of Power Supply H15
28	Live L1	19” Rack Power socket L1
30	Neutral N	19” Rack Power socket N
32	Earth PE	19” Power socket Earth; 19 rack Chassis

7.2.3 Connection of the Sub-D 25 (female)

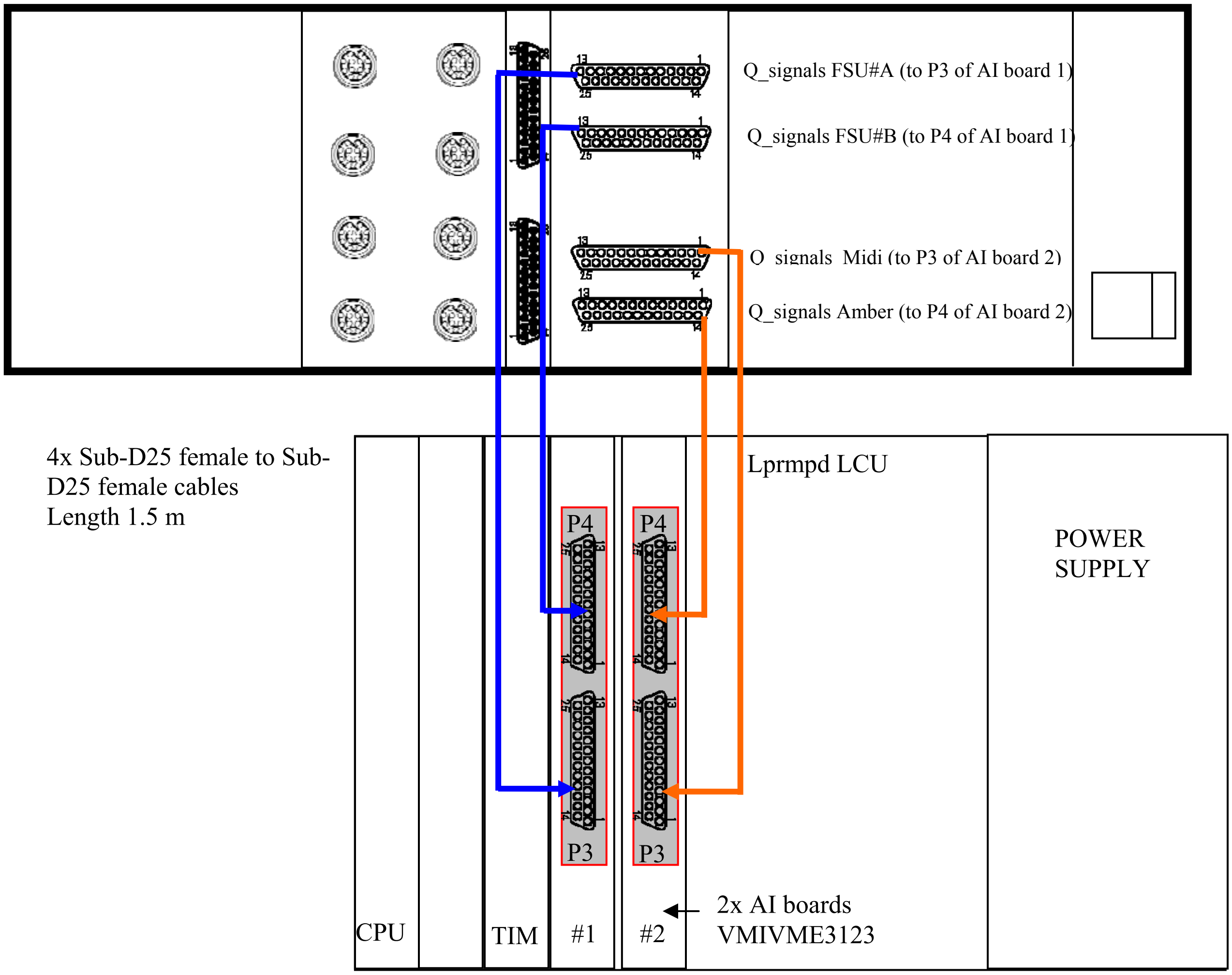
	Description	Pin DIN41612	Pin SubD-25 (female)	Description	Channel nb
X-Beam 2	AGND	Pin 4 Row C	25	Ch7 LO	7
	Q4	Pin 4 Row A	12	Ch7 HI	
			24 connected to 25	Guard (GND)	
	AGND	Pin 3 Row C	11	Ch6 LO	6
	Q3	Pin 3 Row A	23	Ch6 HI	
			10 connected to 11	Guard (GND)	
	AGND	Pin 2 Row C	22	Ch5 LO	5
	Q2	Pin 2 Row A	09	Ch5 HI	
			21 connected to 22	Guard (GND)	
	AGND	Pin 1 Row C	08	Ch4 LO	4
	Q1	Pin 1 Row A	20	Ch4 HI	
			07 connected to 08	Guard (GND)	
X-Beam 1	AGND	Pin 4 Row C	19	Ch3 LO	3
	Q4	Pin 4 Row A	06	Ch3 HI	
			18 connected to 19	Guard (GND)	
	AGND	Pin 3 Row C	05	Ch2 LO	2
	Q3	Pin 3 Row A	17	Ch2 HI	
			04 connected to 05	Guard (GND)	
	AGND	Pin 2 Row C	16	Ch1 LO	1
	Q2	Pin 2 Row A	03	Ch1 HI	
			15 connected to 16	Guard (GND)	
	AGND	Pin 1 Row C	02	Ch0 LO	0
	Q1	Pin 1 Row A	14	Ch0 HI	
			01 connected to 02	Guard (GND)	

X=FSU#A or FSU#B or MIDI or AMBER

Cables from DIN41612 to Pin SubD-25 (female): Twisted pairs

Fixed configuration (hard coded)

CHANNELS	**Analog Input Board/Channels**
Channel A: FSU#A	
Ip1 Quadcell Serial XXXX Beam 1	AI board #1 P3: Q1-Q4=Channels 1-4
Ip3 Quadcell Serial XXXX Beam 2	AI board #1 P3: Q1-Q4=Channels 5-8
Channel B: FSU#B	
Ip2 Quadcell Serial XXXX Beam 1	AI board #1 P4: Q1-Q4=Channels 9-12
Ip4 Quadcell Serial XXXX Beam 2	AI board #1 P4: Q1-Q4=Channels 13-16
Channel A: MIDI	
Ip1 Quadcell Serial XXXX Beam 1	AI board #2 P3 Q1-Q4=Channels 1-4
Ip3 Quadcell Serial XXXX Beam2	AI board #2 P3 Q1-Q4=Channels 5-8
Channel A: AMBER	
Ip1 Quadcell Serial XXXX Beam 1	AI board #2 P4 Q1-Q4=Channels 9-12
Ip3 Quadcell Serial XXXX Beam2	AI board #2 P4 Q1-Q4=Channels 13-16



Q_signals FSU#A (to P3 of AI board 1)
Q_signals FSU#B (to P4 of AI board 1)
O signals Midi (to P3 of AI board 2)
Q_signals Amber (to P4 of AI board 2)
4x Sub-D25 female to Sub-D25 female cables
Length 1.5 m
Lprmpd LCU
POWER SUPPLY
P4
P4
P3
P3
CPU
TIM
#1
#2
2x AI boards
VMIVME3123

7.2.4 Connection of the A0, A1, A10, A11 Digital lines to the SubD-25 (male)

SubD25 (male)	DIN41612 Module X (e.g FSU#A beam 1)
1	A0 (pin 22 row A)
2	A1 (pin 22 row C)
3	A10 (pin 23 row A)
4	A11 (pin 23 row C)
	DIN41612 Module X+1 (e.g FSU#A beam 2)
5	A0 (pin 22 row A)
6	A1 (pin 22 row C)
7	A10 (pin 23 row A)
8	A11 (pin 23 row C)
	DIN41612 Module X+2 (e.g FSU#B beam 1)
9	A0 (pin 22 row A)
10	A1 (pin 22 row C)
11	A10 (pin 23 row A)
12	A11 (pin 23 row C)
	DIN41612 Module X+3 (e.g FSU#B beam 2)
13	A0 (pin 22 row A)
14	A1 (pin 22 row C)
15	A10 (pin 23 row A)
16	A11 (pin 23 row C)
17 n.c	
18 n.c	
19	to Digital GND Bus (pin 30 of all modules) and to Analog_GND
20 n.c	
21 n.c	
22 n.c	
23 n.c	
24 n.c	
25 n.c	

* Set proper jumper on the M58 module to define PIOC4 as GND

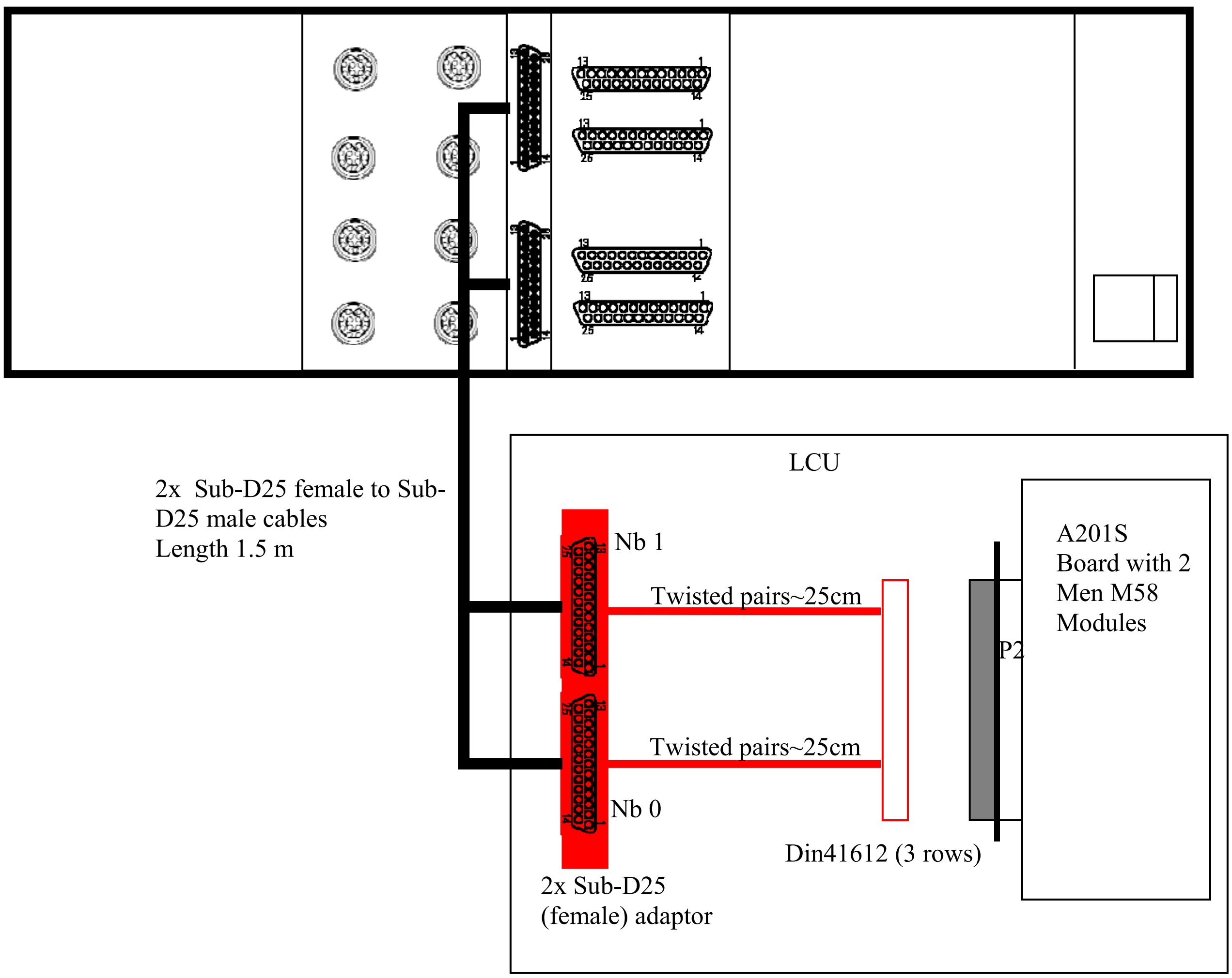
D_GND to be connected to A_GND in the chassis.

The other Sub-D25 is connected to the remaining 4 modules:
e.g. Midi beam 1, Midi beam 2, Amber beam 1, Amber beam 2

Cables from DIN41612 to Pin SubD-25 (male): Twisted pairs

7.3 External Interface cables

7.3.1 Interface cables to 2 Digital Output M-Modules (M58)



2 MEN M58 to be used on a single carrier board:
1 x M58 in Module 0 for FSUA and FSUB: 16 DO + 1 GND
1 x M58 in Module 1 for FSUA and FSUB: 16 DO + 1 GND
D_GND connected to A_GND inside the quadcell chassis.

M58 for FSUA and FSUB: 16 DO + GND (C4) on Module 0			
DIN 41612 3 rows (P2 of M58)	**Digital Output of Module 0**	**SubD25 (female) Nb 0**	**DIN41612 Module X (e.g FSU#A beam 1)**
A25	POA0	1	A0 (pin 22 row A) PGA
B25	POA1	2	A1 (pin 22 row C) PGA
C25	POA2	3	A10 (pin 23 row A) Transimp
A26	POA3	4	A11 (pin 23 row C) Transimp
			DIN41612 Module X+1 (e.g FSU#A beam 2)
B26	POA4	5	A0 (pin 22 row A) PGA
C26	POA5	6	A1 (pin 22 row C) PGA
A27	POA6	7	A10 (pin 23 row A) Transimp.
B27	POA7	8	A11 (pin 23 row C) Transimp
			DIN41612 Module X+2 (e.g FSU#B beam 1)
C27	POB0	9	A0 (pin 22 row A) PGA
A28	POB1	10	A1 (pin 22 row C) PGA
B28	POB2	11	A10 (pin 23 row A) Transimp.
C28	POB3	12	A11 (pin 23 row C) Transimp
			DIN41612 Module X+3 (e.g FSU#B beam 2)
A29	POB4	13	A0 (pin 22 row A) PGA
B29	POB5	14	A1 (pin 22 row C) PGA
C29	POB6	15	A10 (pin 23 row A) Transimp.
A30	POB7	16	A11 (pin 23 row C) Transimp
		17 n.c	
		18 n.c	
C31	PIOC4 (GND; set Jumper !)	19	
		20 n.c	
		21 n.c	
		22 n.c	
		23 n.c	
		24 n.c	
		25 n.c	

* Set proper jumper on the M58 module to define PIOC4 as GND

M58 for AMBER and MIDI: 16 DO + GND (C4) on Module 1			
DIN 41612 3 rows (P2 of M58)	**Digital Output Of Module 1**	**SubD25 (female) Nb 1**	**DIN41612 Module X (e.g MIDI beam 1)**
A17	POA0	1	A0 (pin 22 row A) PGA
B17	POA1	2	A1 (pin 22 row C) PGA
C17	POA2	3	A10 (pin 23 row A) Transimp
A18	POA3	4	A11 (pin 23 row C) Transimp
			DIN41612 Module X+1 (e.g MIDI beam 2)
B18	POA4	5	A0 (pin 22 row A) PGA
C18	POA5	6	A1 (pin 22 row C) PGA
A19	POA6	7	A10 (pin 23 row A) Transimp.
B19	POA7	8	A11 (pin 23 row C) Transimp
			DIN41612 Module X+2 (e.g AMBER beam 1)
C19	POB0	9	A0 (pin 22 row A) PGA
A20	POB1	10	A1 (pin 22 row C) PGA
B20	POB2	11	A10 (pin 23 row A) Transimp.
C20	POB3	12	A11 (pin 23 row C) Transimp
			DIN41612 Module X+3 (e.g AMBER beam 2)
A21	POB4	13	A0 (pin 22 row A) PGA
B21	POB5	14	A1 (pin 22 row C) PGA
C21	POB6	15	A10 (pin 23 row A) Transimp.
A22	POB7	16	A11 (pin 23 row C) Transimp
		17 n.c	
		18 n.c	
C23	PIOC4 (GND; set Jumper !)	19	
		20 n.c	
		21 n.c	
		22 n.c	
		23 n.c	
		24 n.c	
		25 n.c	

* Set proper jumper on the M58 module to define PIOC4 as GND

7.3.2 Interface cables to Analog Input boards VMIVME3123

Quantity : 4
Length: 2 meters
Connectors: SubD25 (male); SubD25 (male)
Pin Plan: “one to one”
Type of cable: Twisted pair; Shielded ; (no flat cable); shield connected to the connector case on both sides.

8 APPENDIX 1: NOTES FROM THE PROTOTYPING RESULTS.

Saturation level of transimpedance amplifier
S=0.9 A/W ;Rf=1MOhm;Vmax(OPA2380)= (4.3-0.7)=3.6 V
Vmax=Rf.i=Rf.S.Pmax-> Pmax=3.6/1e6/0.9=4µW

The saturation level of the PGA204 is about Vsat=10 V.
For G=1, Vmax=3.6V is fully transmitted by the PGA204.
The saturation level of each Q is given by the OPA2380 i.e Vmax=3.6 V or Pmax=4µW
The saturation level of 4 quadrants is 4x4µW=16µW
For a centered spot, the saturation of the sum (10V) occurs for each Q=Vsat/4=2.5 Volts (instead of 3.6 V), i.e for a total of 4x Pmax.(Vsat/Vmax)*4= 11.1 µW

For G=10, Vmax=3.6V is amplified by x10 and limited to Vsat=10V !
The saturation level of each Q is now given by the PGA204, i.e for Vpga_out=Vsat=10V, thus P=Pmax*Vsat/(Vmax.G)= 1.1 µW. For a centered spot, the saturation of the sum occurs for the same power.

For G=100, Vmax=3.6V is amplified by x100 and limited to Vsat=10V !
The saturation level of each Q is now given by the PGA204, i.e for Vpga_out=Vsat=10V, thus P=Pmax*Vsat/(Vmax.G)= 111 nW. For a centered spot, the saturation of the sum occurs for the same power.

	Saturation level Vsat=10V	Saturation level Vsat=12V
G=1	4 µW per Q, i.e =16 µW or 11.1 µW on the sum (centered spot)	4 µW per Q, i.e =16 µW or 12 µW on the sum (centered spot)
G=10	1.1 µW	1.2 µW
G=100	111 nW	122 nW

Note: Due to the attenuation of the filter transfer function, Vsat=11 V can appear at the output at V<Vsat, but the power scaling should be done on the saturation level of the PGA, i.e Vsat=11V

For G=1, a saturation of a single Q can occur before the saturation of sum:
(exemple: Q1=3.6 Volt, Q2=Q3=Q4=1V). If the spot moves towards Q1, Q1 will not increase anymore due to saturation, but Q2 to Q4 will decrease and the sum will globally decrease, leading to a measurement error. For G=1, it is important to practically verify that each Q do not saturates before to monitor the sum and try to compute the displacement.

Measured voltage/position sensitivity for displacement along X and Y:
50mV/ µm for a φ=400µm diameter spot. (this sensitivity depends only on the spot diameter and not on the gain)
->we expect 20mV/µm for a beam diameter of φ=1mm.

Simulation:
10 nW per quadrant (40 nW total), EOS, OPA380-> rms position error<0.1 µm
Analog input board: noise close to quantification noise 300 µV

9 APPENDIX 2: PIN PLAN OF THE VMIVME3123 AI BOARD

Differential input pairs.For some input signals, it may be necessary to connect Guard to LO. It is absolutely necessary for isolated input signal sources.

AI board VMIVME3123 **P3** Pin Assignments (SubD25 Female front connector)		
Pin Number	Signal	Channel
13	Analog GND	
25	Ch7 LO	7
12	Ch7 HI	
24	Guard (GND)	
11	Ch6 LO	6
23	Ch6 HI	
10	Guard (GND)	
22	Ch5 LO	5
09	Ch5 HI	
21	Guard (GND)	
08	Ch4 LO	4
20	Ch4 HI	
07	Guard (GND)	
19	Ch3 LO	3
06	Ch3 HI	
18	Guard (GND)	
05	Ch2 LO	2
17	Ch2 HI	
04	Guard (GND)	
16	Ch1 LO	1
03	Ch1 HI	
15	Guard (GND)	
02	Ch0 LO	0
14	Ch0 HI	
01	Guard (GND)	

AI board VMIVME3123 **P4** Pin Assignments (SubD25 Female front connector)		
Pin Number	Signal	Channel
13	Analog GND	
25	Ch15 LO	15
12	Ch15 HI	
24	Guard (GND)	
11	Ch14 LO	14
23	Ch14 HI	
10	Guard (GND)	
22	Ch13 LO	13
09	Ch13 HI	
21	Guard (GND)	
08	Ch12 LO	12
20	Ch12 HI	
07	Guard (GND)	
19	Ch11 LO	11
06	Ch11 HI	
18	Guard (GND)	
05	Ch10 LO	10
17	Ch10 HI	
04	Guard (GND)	
16	Ch9 LO	9
03	Ch9 HI	
15	Guard (GND)	
02	Ch8 LO	8
14	Ch8 HI	
01	Guard (GND)	