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VERY LARGE TELESCOPE

Technical Specification and Statement of Work for the Design of the Phase Meter of the PRIMA Metrology System

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1 Scope

This document defines the technical specification and statement of work for the design of the Phase Meter of the PRIMA metrology system.

2 Applicable Documents

AD 1 Technical Specifications for the PRIMA Metrology System, VLT-SPE-ESO-15730-2211, Issue 1, 16/10/00.

AD 2 Optical Phase Detector Unit for the PRIMA Metrology, Design Review, VLT-TRE-IMT-15734-0002, 20/11/00

AD 3 PMC-HPDI32, 32-bit High Speed Parallel Digital Interface, User manual, www.generalstandards.com

AD 4 Time reference system, Time interface module, Technical Manual, VLT-MAN-ESO-17300-473, Issue 2, 11/7/95.

AD 5 Interface Control Document between VLTI and its instruments, VLT-ICD-ESO-15000-1826, Issue 3.0, 15/02/02

AD 6 VLT electronic design specifications, VLT-SPE-ESO-10000-0015, issue 4, 9/12/96

AD 7 Electromagnetic compatibility and power quality specifications, part 2: electromagnetic disturbance emission and immunity limits of electric and electronic equipment, VLT-SPE-ESO-10000-0003, issue 1, 5/2/92.

AD 8 Acceptance procedure electrical safety and EMC, VLT-VER-ESO-10000-0958, issue 2, 1/3/96.

3 Acronyms

- AD: Applicable Document
- AOM: Acousto-Optics Modulator
- EMC: Electromagnetic Compatibility
- FDR: Final Design Review
- HW: Hardware
- LCU: Local Control Unit
- PM: Polarization maintaining
- KO: Kick Off
- RD:Reference Document
- PRIMA:Phase Referenced Imaging and Micro-arcsec Astrometry

- RD:Reference Document
- RMN:Reflective Memory Network
- SW: Software
- TBC:To Be Confirmed
- TBD:To Be Defined
- TIM:Time Interface Module
- WP: Work Package

4 System Definition and Implementation Baseline

The Phase Meter is an opto-electronic system mounted on VME boards required to detect and process the interference signals generated by the two channels of the PRIMA Metrology system. Its role is to measure the phase difference between these signals, as defined in AD 1 and make it available to the Metrology LCU.

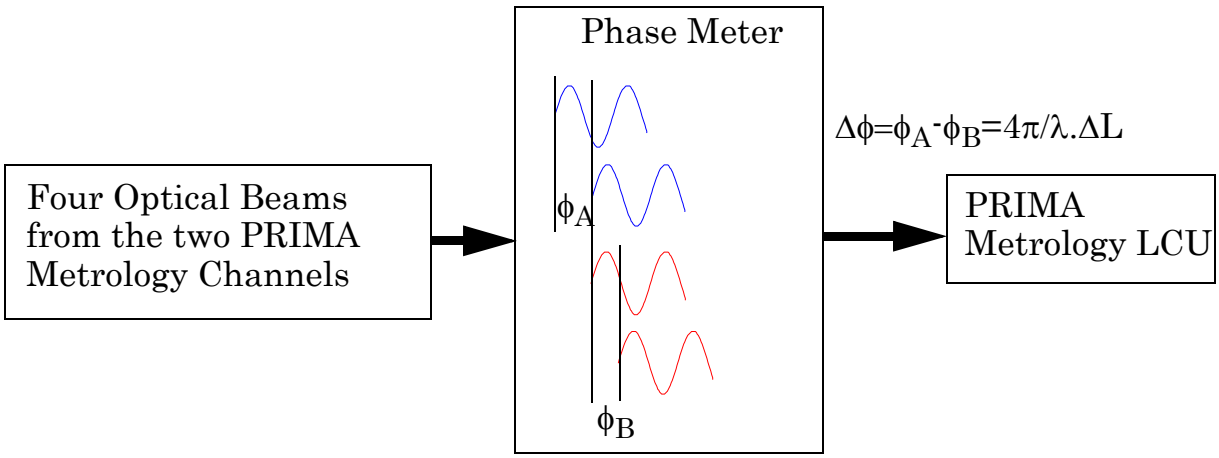

Figure 1 Functional sketch of the Phase meter

The design of the Phase Meter shall be based on the prototype developed by the Institute of Micro-technology of Neuchâtel, AD 2. All heterodyne frequencies as well as the operating wavelength used by the prototype remain applicable:

- Heterodyne frequency for channel A: 450 kHz
- Heterodyne frequency for channel B: 650 kHz
- Super-heterodyne frequency: 200kHz
- Operating wavelength: λ=1319nm

Because the PRIMA metrology system will be implemented in a double-pass configuration, a $\Delta\phi=2\pi$ differential phase measured by the Phase Meter will correspond to a differential optical path of $\Delta L=\lambda/2$.

Upon reception of a trigger signal from the TIM board of the metrology LCU, the Phase Meter shall deliver at its P2 output the measured phase as well as status data as described in section 5.

The Phase Meter will be connected via its P2 connector to a fast digital input board HPDI32 mounted on the Slave CPU of a Master/Slave dual CPU system (see Fig. 3). The HPDI32 is a PMC board running 32 bits transfer at a rate of up to 25 MHz, AD 3. It includes a 64Kbytes FIFO buffer.

The role of the slave CPU is to process the data and status delivered by the Phase Meter. This includes the following tasks: average and convert ΔL in meters, generate a validation flag, write ΔL to the Reflective Memory Network, store ΔL with a proper time stamp.

5 Technical Specifications

5.1 System performance

The following performance applies to the photodetection & phase measurement chain:

- Resolution: $2\pi/1024$ rad (or 0.64 nm)
- Internal Sampling Frequency: F_{s_int}=200kHz
- Standard Deviation of the noise: < Resolution for an optical power >100nW per interferometric arm and a fringe visibility of V=70%
- Accuracy: $<2\pi/800$ rad (or 1.2 nm) for an optical Power of 20nW per interferometric arm and a fringe visibility of V=70% and a 50kHz Bandwidth.
- Bandwidth: B=110kHz for each interferometric channel (i.e ±55 kHz centered on their respective heterodyne frequency) and B=55 kHz for ΔL (i.e ±27.5 kHz centered on F_{s_int}=200kHz).

5.2 Data Transfer

Upon reception of a trigger signal from the TIM board of the metrology LCU, the Phase Meter shall deliver at its P2 output a sequence of 32 bits words, each preceded by a Strobe signal. These words are:

The sum of the differential phases,

recorded since the previous trigger signal[1]: $\Phi_N = \sum_{i=1}^{N} \Delta\phi_i$

Each $\Delta\phi_i$ represents the differential phase recorded at a sampling frequency F_{s_int}. $\Delta\phi_i$ shall be coded on 32 bits and expressed in "multiple of resolution step in rad"[2]. Φ_N shall be coded on 64 bits and transferred in 2 packets of 32 bits.

The effective number of valid samples,

N, integer, 32 bits long

The value of the corrected phase,

ϕ_c (see definition in AD 2), expressed in "multiple of resolution step in rad", 32 bits long.

The status information,

64 bits sent in 2 packets of 32 bits (see definition in section 5.3).

The delay, δ, between the time when the trigger is received by the Phase Meter and the time when the first 32 bits word is available on the P2 connector shall not exceed 1 µsec (see Figure 2). Similarly the period, τ, for the transfer of two 32 bits words shall not exceed 1 µsec

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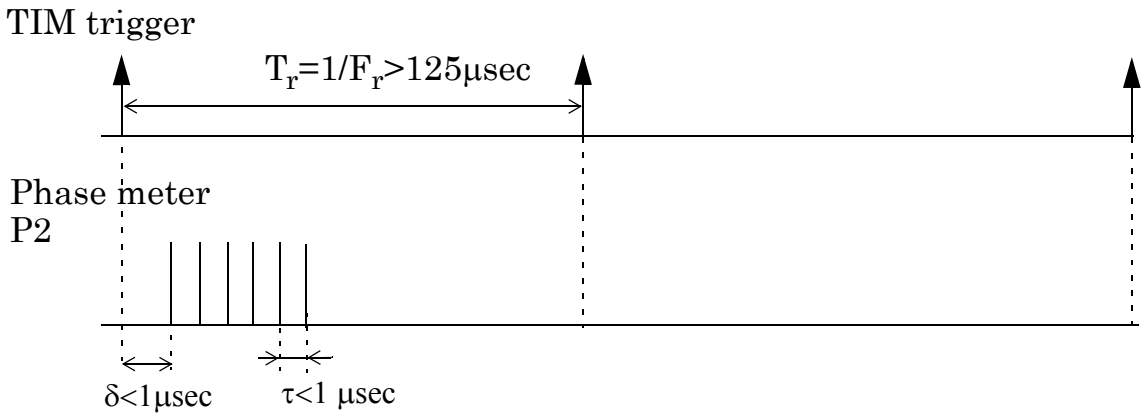

Figure 2 Timing for the transfer of the six 32 bits words.

In case of problem during a phase measurement (e.g. temporary loss of flux), N should not be incremented and $\Delta\phi_i$ should be discarded. The status should reflect the nature of the problem (see Table 1).

5.3 Status

Upon receiving a trigger signal, the phase meter shall provide the status information listed in Table 1.

Table 1 List of status

Description	Number of bits required
Status of Interferometric signals (AC components)	

1. The trigger signal will have a period ranging from T_r=125 µsec to 2 sec by steps of 125 µsec
2. Also referred as DIGIT

Table 1 List of status

Description	Number of bits required
450 kHz ref signal detected	1
450 kHz probe signal detected	1
650 kHz ref signal detected	1
650kHz probe signal detected	1
200kHz probe signal detected	1
Phase-lock Loop operating	1
Signal level of Photodiodes:	
DC level of Photodiode 1	8
DC level of Photodiode 2	8
DC level of Photodiode 3	8
DC level of Photodiode 4	8
Overflow of counters	
Integer counter of $\Delta\phi_i$ overflow	1
Integer counter of ϕ_c overflow	1
Trigger	
Trigger signal detected	1
Reset	
Reset detected	1
Spare bits for additional status	22
	Total: 64

5.4 Reset of the phase meter

Upon receiving a reset signal from the TIM, the phase meter shall internally zero the following current measurements within 5 μsec:

- The phase and corrected phase, $\Delta\phi_i$ and ϕ_c
- The summed phase, Φ_N
- The number of samples, N

5.5 Hardware requirements

The Phase Meter shall be integrated on 6HE VME boards. In order to facilitate replacement and repair, several boards shall be used with well separated functions as in the Phase Meter prototype. This includes:

- Photodetection board
- Super-heterodyne Board
- Interface board
- Digital Phase meter Board
- Digital status board

The Phase Meter shall include all front panel test points available on the prototype. The output of the photodetectors shall be DC coupled.

The design of the Phase Meter shall comply with the ESO Electronic Design Specification, AD 6, as well as with the electromagnetic emission limits defined in AD 7. EMC guidelines are summarized in section 7. The design of the Phase Meter shall include all means necessary to preclude or limit hazards to personnel and equipment during assembly, disassembly, maintenance, test and operation.

All exchangeable boards shall be equipped with nameplates containing the following information:

- Board name and reference number
- Date of manufacturing
- Name of manufacturer

5.6 Interface definition and requirements

5.6.1 Allocated space

All the boards of the Phase meter shall be mounted inside a dedicated VME Crate and use a maximum of 12 consecutive slots (design goal). The phase meter will be integrated in the PRIMA metrology electronic cabinet.

5.6.2 Electrical power and Signals interface

Each board of the Phase Meter shall be powered using the ±12V voltage available on the P1 backplane of the VME crate.

The trigger and reset signals will be provided by the TIM board (TTL compatible level, negative logic), AD 4. The frequency of the trigger signal will range from F_r=0.5 Hz to 8kHz. The reset signal will be a pulse with a minimum width of 1 μsec.

In order to match the PMC-HPDI32 interface, all data and status shall be available on a single 64 pins connector (type Robinson Nugent #P50E-080-S-TG using differential line Drivers for proto-

col RS422/485, AD 3. The strobe signals shall be compatible with the specifications defined in AD 3.

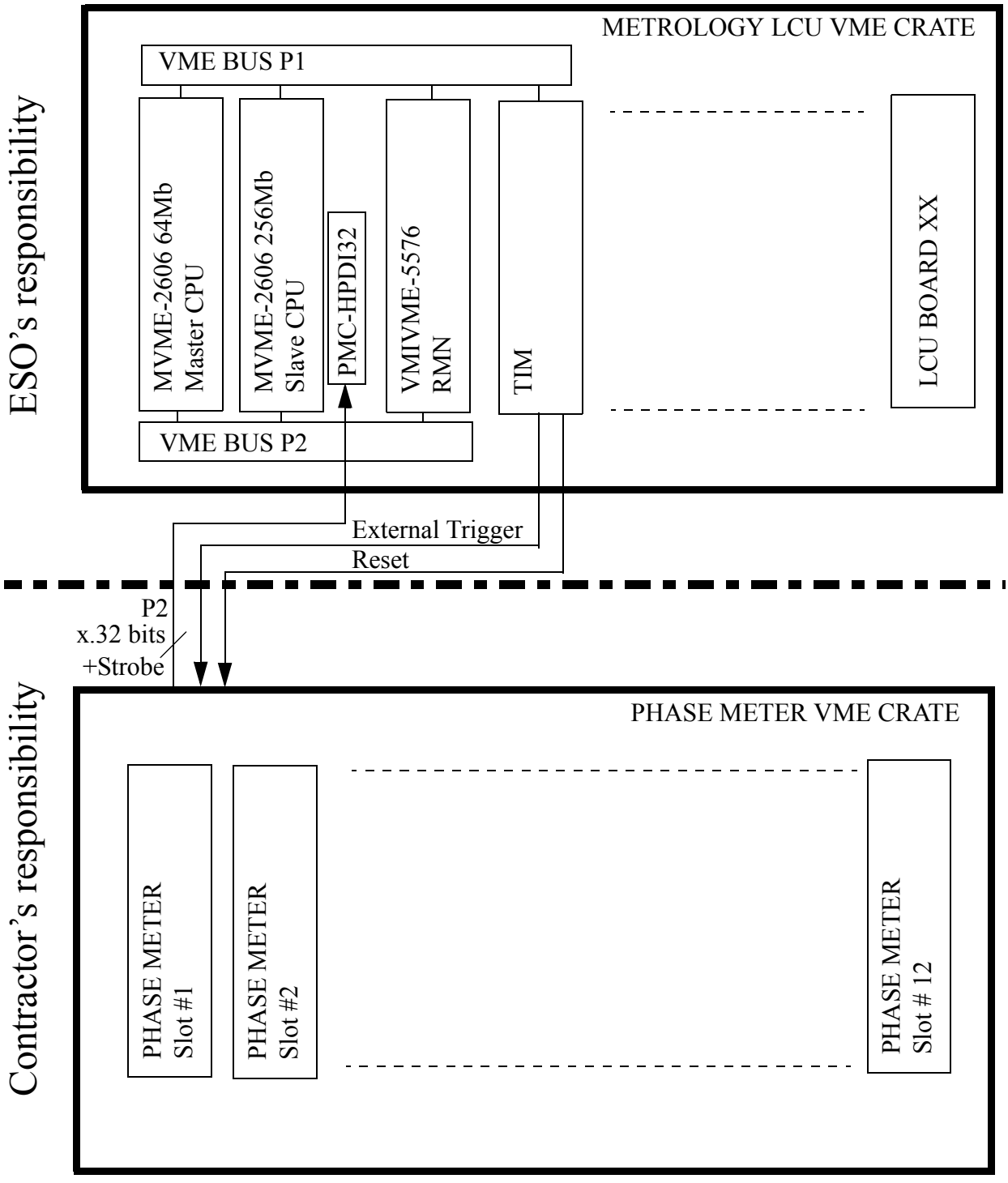

Figure 3 Allocated space and interface to the metrology LCU.

5.6.3 Interface with the PRIMA Metrology Beams

The metrology beams will be delivered to the phase meter through optical fibers mounted with FC connectors (2 mm key). Four metrology beams will input the Phase Meter:

- For Channel A: one reference signal and one probe signal: wavelength λ=1319nm, beat frequency 450kHz,
- For Channel B: one reference signal and one probe signal: wavelength λ=1319nm, beat frequency 650kHz

5.6.4 Environmental conditions and Thermal dissipation requirements

The phase meter will be used in a temperature controlled environment (17 ºC ± 2 ºC). According to AD 1, the power dissipated by the overall PRIMA Metrology equipment shall be less than 1kW. During the Design phase, a thermal budget shall be elaborated for the Phase Meter. It will be used as an input to the PRIMA Metrology thermal budget.

5.7 Reliability and Maintainability

The reliability requirements defined in AD 1 apply to the Phase Meter. All necessary spare boards shall be defined to fulfil these requirements. The Phase Meter shall be designed to avoid any maintenance work at Paranal.

5.8 Product Assurance requirements

The product assurance strategy described in AD 1 shall be applied to the Phase Meter. In particular, this includes the definition of a verification plan based on Table 2. Test procedures shall be defined. This includes the acceptance tests, which shall provide evidence that all functional and performance requirements are met.

Table 2 Verification matrix of the Phase Meter during the design phase

Requirements	Verification by	
	Design	**Analysis**
Technical Specifications		
System performance	x	x
Data Transfer	x	x
Status	x	x
Reset of the phase meter	x	x
Interface definition and requirements	x	x
Hardware requirements	x	x
Reliability and Maintainability	x	x

6 Statement of Work

6.1 Introduction

The contractor shall perform all tasks necessary for the Design of the Phase Meter in accordance with the present document. All tasks shall be defined the workpackage WP3240. A preliminary Workpackage definition is given in Table 4

6.2 Project Phases and Reviews

The project includes a Design Phase concluded by a Final Design Review.

6.3 Project Milestones Summary

Table 3 Milestones

Milestones	Acronym	Schedule	Location of meeting
Kick Off Meeting	KO	T0	Contractor's premises
Final Design Review	FDR	T0+3 months	ESO Garching

6.4 Reporting and meetings

The project reporting shall be based on the following types of reports and meetings:

- A Monthly Progress Report prepared by the contractor including an update of the schedule and the status of the tasks defined in the Workpackage WP3240.
- One Progress Meeting held at the contractor's premises or at ESO Garching.
- Project Review Reports.
- One Final Design Review meeting held at ESO Garching.

Problems shall be reported in the form of Red Flag reports, Request for Waiver or Change Request.

6.5 Documentation

The following numbering scheme shall be used by the Contractor for all documents related to the Phase Meter project.

VLT-BBB-CCC-15734-GGGG

where:

· BBB identifies the type of document (see list below)

· CCC is the code for the Firm or Organization issuing the document (given by ESO)

· 15734 is the product code number of the Phase Meter

· GGGG is a sequential identification number (including preceding zeros)

The document type codes (BBB) are defined as follows:

· CRE:Change Request

· DWG:Drawings

· MIN:Minutes of Meeting

· PLA:Plan

· RFW:Request for Waiver

· TRE:Technical Report

6.6 Deliverable

The contractor shall deliver the complete FDR data package such that the manufacturing of the phase meter can start immediately after the FDR. The deliverable also includes the source code of the Programmable Logic Components. The FDR data package shall be sent to ESO for review one week before the FDR meeting date.

Table 4 Definition of WP 3240

Project: Prima Metrology **WP 3240 Phase Meter** **WP Manager: TBD** **Contractor: TBD** **Start: KO** **End: FDR**
Inputs PRIMA Metrology Technical specifications (VLT-SPE-ESO-15730-2211) Technical Specification and Statement of Work for the Design of the phase meter (VLT-SPE-ESO-15734-2921)
Task Description Design of the phase meter based on the technical specification and on the results of the phase meter prototype developed in 2001 by the Institute of Microtechnology of Neuchâtel. Preparation of the FDR data package.
Outputs FDR data package (design and analysis reports, manufacturing drawings, test and verification plan, spare part list; preliminary installation and operation manuals).
Resources To be completed by the contractor

7 Appendix: EMC Cook-book

The following guidelines shall be used for the EMC design:

-EMC Design from the beginning

-Partition of the system into critical and non-critical sections

- determine which circuits will be noisy or susceptible and which will be not
- lay them out in separate areas as far as possible
- separate digital and analogue systems
- select internal and external interface points to allow optimum common-mode current control

- Select components and circuits with EMC in mind

- use slow (as slow as possible) and/or high immunity logic
- -minimize rise/fall times on signal and clock edges

- use good RF decoupling, close to the origin
- -use low impedance capacitors (e.g. ceramic multi layer)
- minimise signal bandwidth, maximise levels
- -use low pass filters
- minimise output drive from clock circuits
- -provide power supplies of adequate (noise-free) quality
- consider a watchdog circuit on every microprocessor
- use Surface Mounted Devices (SMD) where possible

- **PCB layout**
  - track all signal lines on the board, avoid 'flying leads' across the board
  - ensure proper signal returns; if necessary include isolation to define preferred current paths
  - keep interference paths segregated from sensitive circuits
  - minimise ground inductance with thick girding or ground plane(s), use power plane where possible
  - minimise enclosed loop areas in high current, high di/dt or sensitive circuits
  - minimise surface areas of nodes with high dv/dt
  - minimise HF and RF track length and component leadout lengths
  - use wide tracks for power lines and decoupage at local boundaries(use low Q RLC filters), avoid overlapping power planes
  - if possible make tracking run orthogonal between adjacent layers
  - use track mitring (bevelling the edges at corners), and avoid track stubs
  - do not leave any floating conductor areas, if possible connect to ground plane
  - on sensitive components and termination use surrounding guard rings and ground fill, where possible (only connect the guard ring to the ground at a single point and make no other use of it)
  - avoid slit apertures in the PCB layout, particularly in ground planes or near current paths

- **Cables**
  - avoid parallel runs of signal and power cables
  - use signal cables and connectors with adequate screening
  - use twisted pair if appropriate
  - run cables away from apertures in the shielding, close to conductive grounded structures
  - avoid resonant lengths (close to the quarter wavelength of the signal frequency) where possible, consider damping cables with ferrite suppressers

- ensure that cable screens are properly terminated to the correct type of connector
- where possible, try to keep all I/O cables in one area
- ensure filtering of cables and over voltage protection at the termination, especially for cables external to the system (if possible isolate the signals using e.g. fibre optic cable)

- **Grounding**
  - design and enforce the ground system at the product definition stage
  - consider the ground system as a return current path, not as 0 V reference
  - ensure adequate bonding of screens, connectors, filters, cabinets, etc.
  - ensure that bonding methods will not deteriorate
  - mask paint from any conductive areas
  - keep earth leads short and define their geometry
  - avoid common ground impedance
  - provide a clean ground area for decoupling all interfaces

- **Filters**
  - optimise the main filters for the application
  - use correct components (SMD where possible) and filter configuration for I/O lines
  - ensure a good ground return for each filter
  - apply filtering to interference sources, such as switches or motors
  - pay attention to the layout of filter components and associated wiring or tracks

- **Shielding**
  - determine the type and extent of shielding required from the frequency of range
  - enclose fast switching circuits, main power supply components, low power circuitry and particularly sensitive or noisy areas with extra internal shielding where possible
  - avoid large or resonant apertures in the shield, or take measures to mitigate them
  - ensure that separate panels are well bonded along their seams

-Test and evaluate for EMC continuously as the design progresses

- emission
- -fields
- -conducted
- immunity
- -electrostatic discharge (ESD)

- -surge
- -burst (also called Electrical Fast Transients, EFT)
- -fields
- -voltage variations