



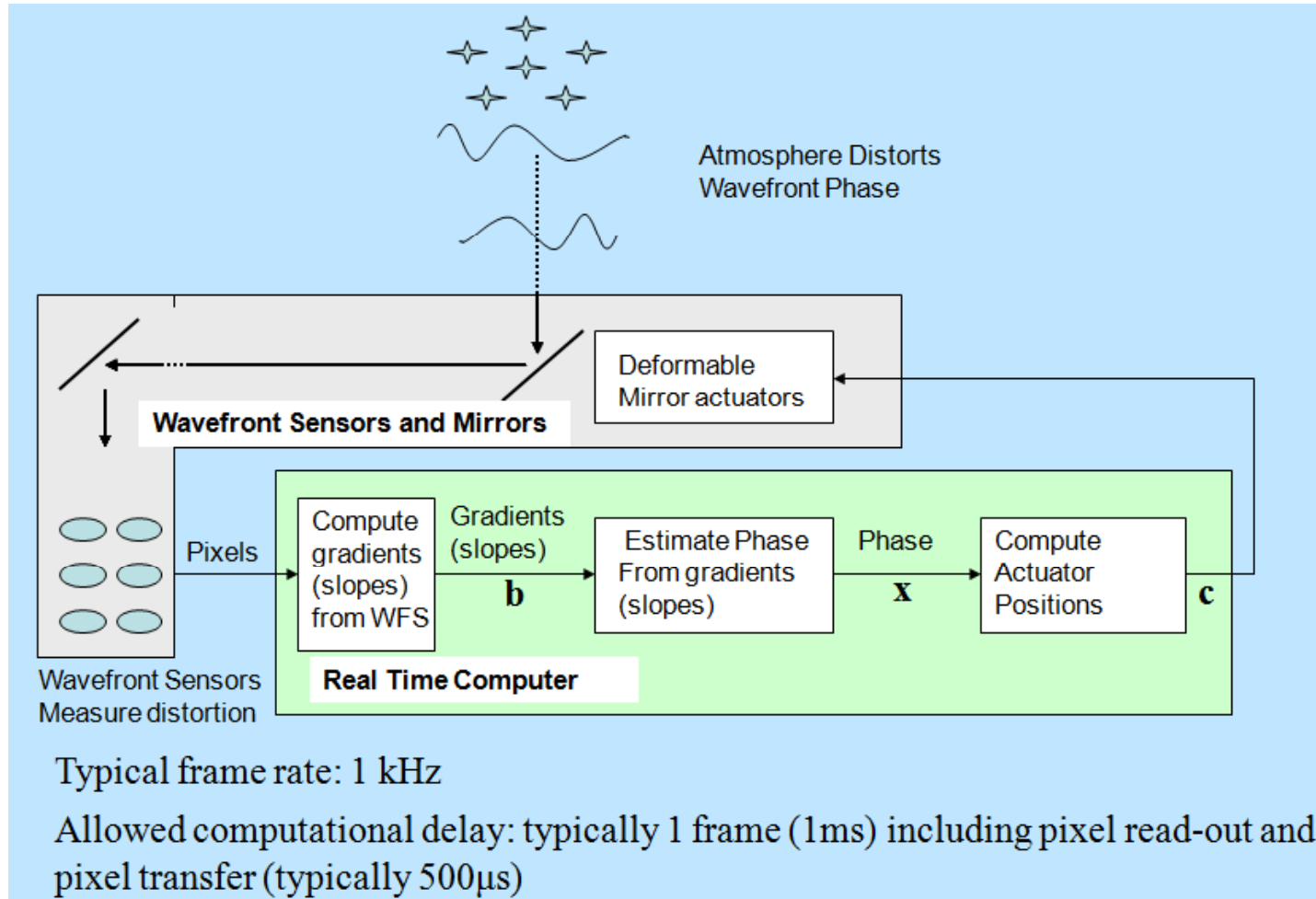
Munich AO RTC Workshop
ATCA Based AO RTC
Zoran Ljusic
December 2012



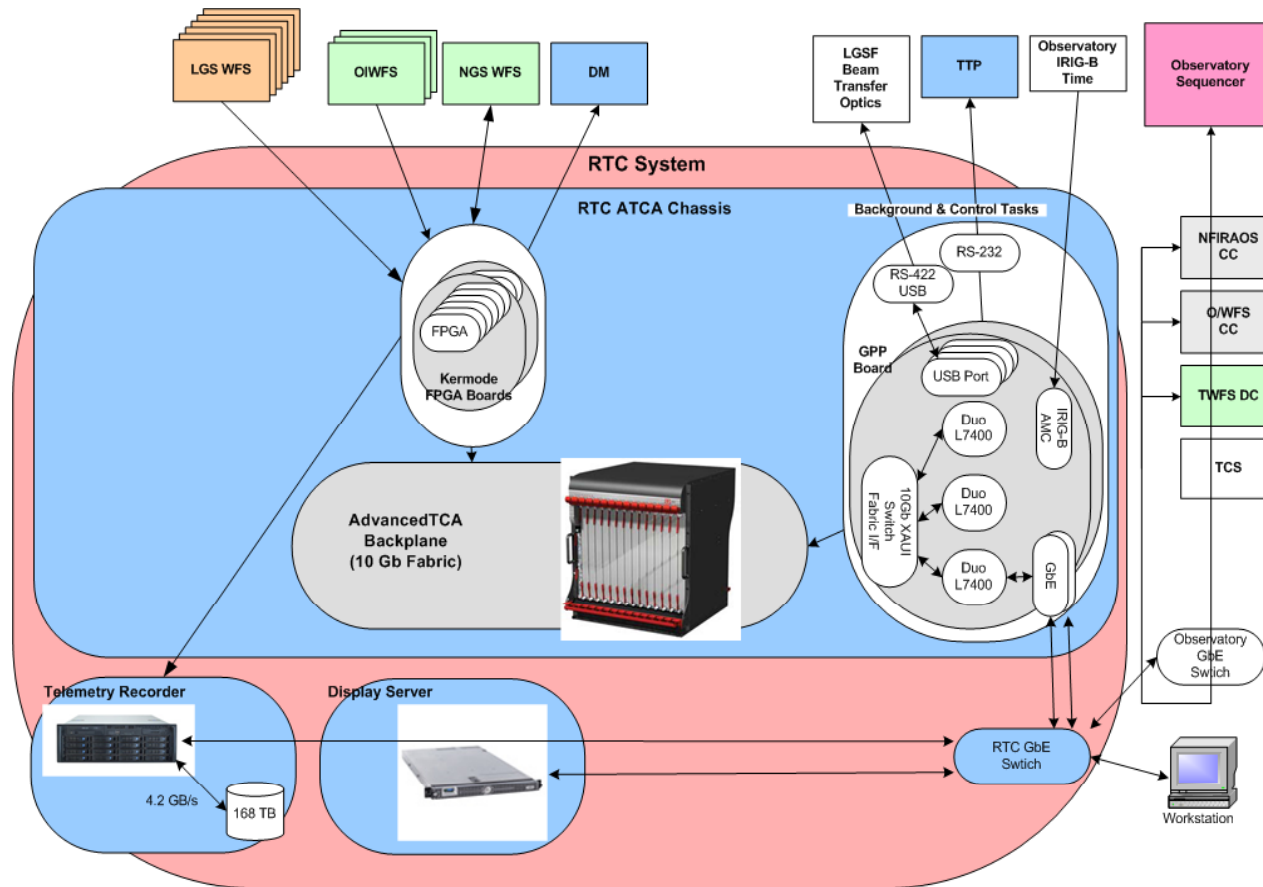
Outline

- NFIRAOS system
- ATCA System outline
- Kermode FPGA board
- Pixel Processing
- MVM
- CG
- FD CG
- New FPGA generation

Simplified NFIRAOS diagram



TMT RTC block diagram



The proposed solution for the Real Time Computer within NFIRAOS for TMT project is ATCA based system with an FPGA processing board.

ATCA System Outline

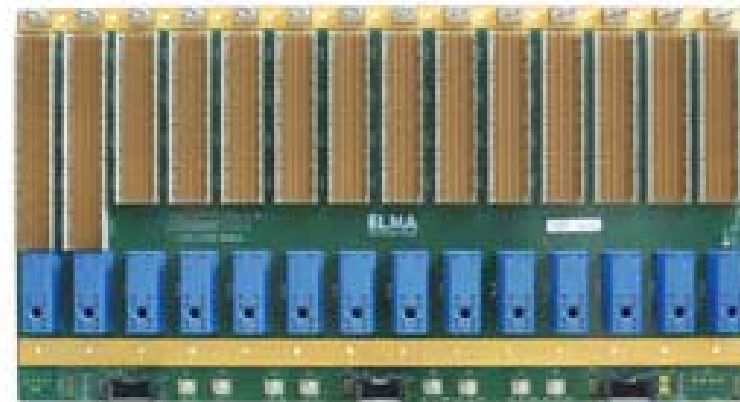
- Advanced Telecom Computing Architecture, ATCA, is designed to be used in central office grade equipment.
- The ATCA specification V3.0 by PCI Industrial Computer Manufacturers Group, PICMG, defines the chassis form factor, back plane, boards, power..
- Many possible applications where high volume data need to be processed fast.
- It can be used in Radio Astronomy and Adaptive optics.
- Many modules available off-the-shelf, COTS.

ATCA system



ATCA shelf with cooling fans

- Different sizes available, 6, 14 and 16 slots systems Common.



14 slot back plane

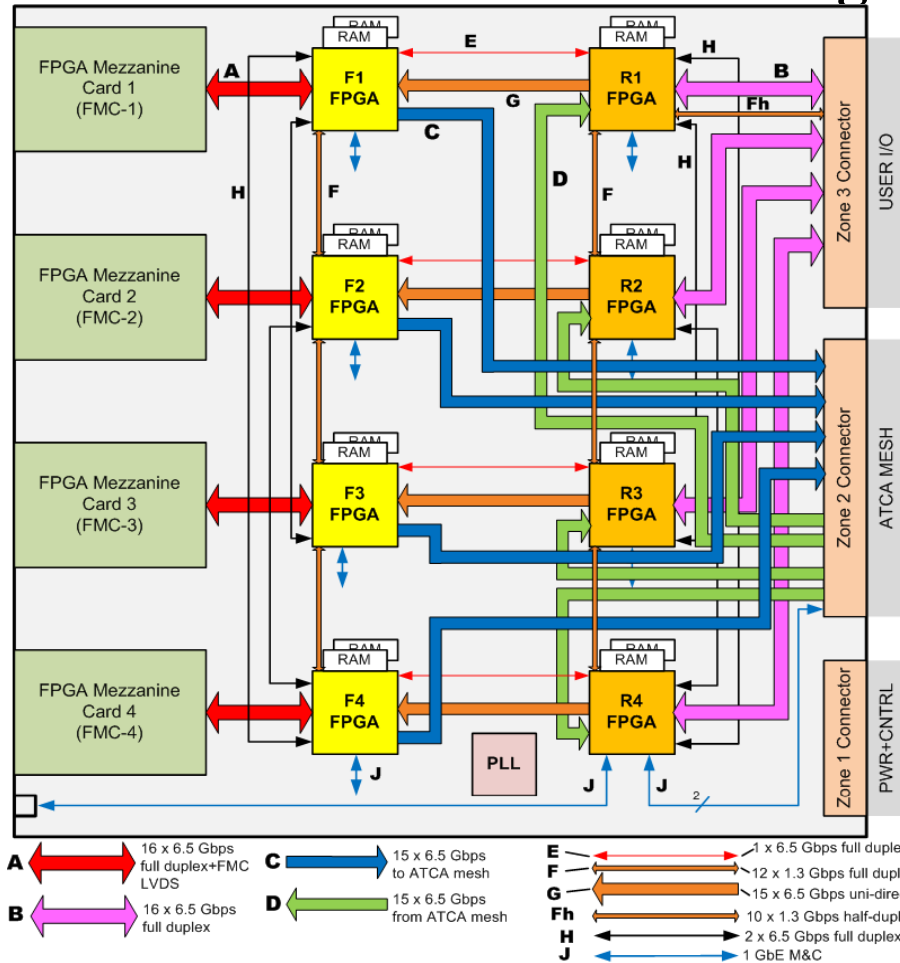
Back planes provide:

- Power via -48V rails
- Control and data signals
- Full-mesh between boards at 10 Gbps
- Kermode based system 20 Gbps

Kermode ATCA board

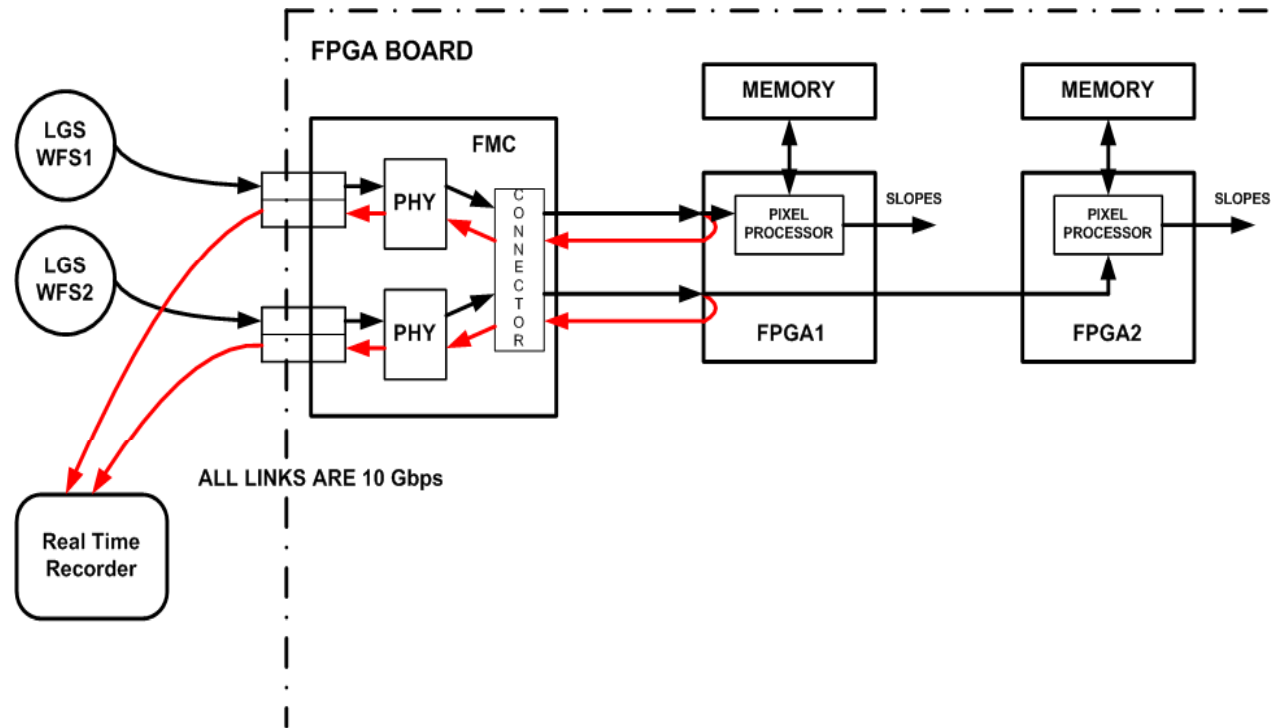
- The Kermode board was primarily developed for use in Radio Astronomy and Adaptive Optics.
- In Radio Astronomy the Kermode based ATCA computing system could be used perform a variety of DSP tasks such are:
 - Beam former and filter bank
 - Correlator
 - Pulsar binning machine
- In Adaptive Optics the Kermode based ATCA system could be used as a Real Time Computer.
- The Kermode could be ordered thru Canadian company Nutaq (Lyrtech).

Kermode FPGA board connectivity and block diagram



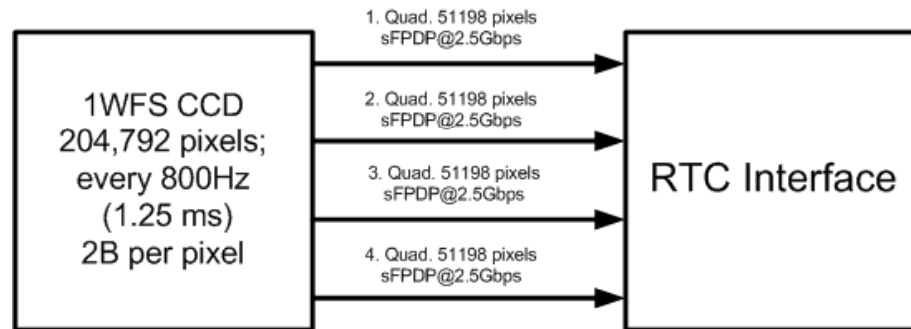
- Standard AdvancedTCA form factor: 280 X 322 mm (11.024" X 12.67").
- High I/O bandwidth : 150Gbps Zone 2; 160Gbps Zone 3
- 8 Xilinx FPGAs (Virtex-6 SX475), 4 F-FPGAs (front column) and 4 R-FPGA (rear column), 1TMACs per FPGA device.
- FMC cards, each connects to an F-FPGA, for flexible I/O interfacing or for additional processing power.
- Each FPGA connects to 2 DDR3 SODIMM modules at 13MB/s memory bandwidth.
- 350W power dissipation.
- Monolithic heat sink

Interfacing with wave front sensors

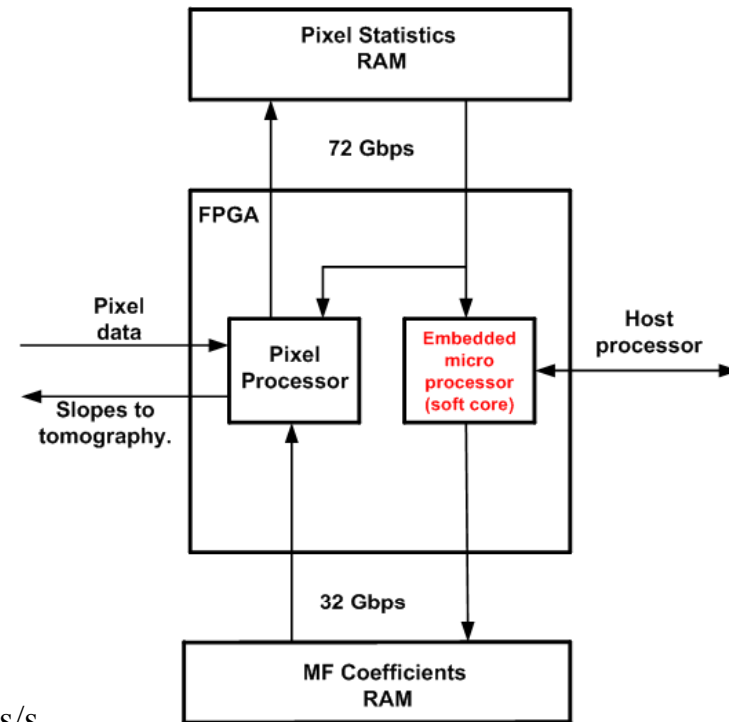


- FPGA1 and FPGA2 belong to the front group of devices. Therefore one Kermode interfaces with 4 WFS.
- WFS data could enter the board:
 - From front side via FPGA Mezzanine Card, FMC.
 - From rear side via Rear Transition Module, RTM.

Pixel Processing



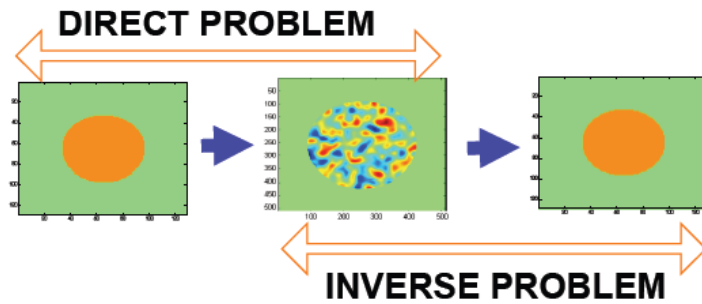
Each WFS is divided in 4 quadrants.
 There are 50 sFPDP data readout frames per quadrant.
 A frame is made of 1024 2 byte pixels data plus header.
 To transfer one data frame takes 8.3 μ s, which is 123.45 MWords/s,
 or 246.9 MB/s or approx 2Gbp/s effective pixel rate



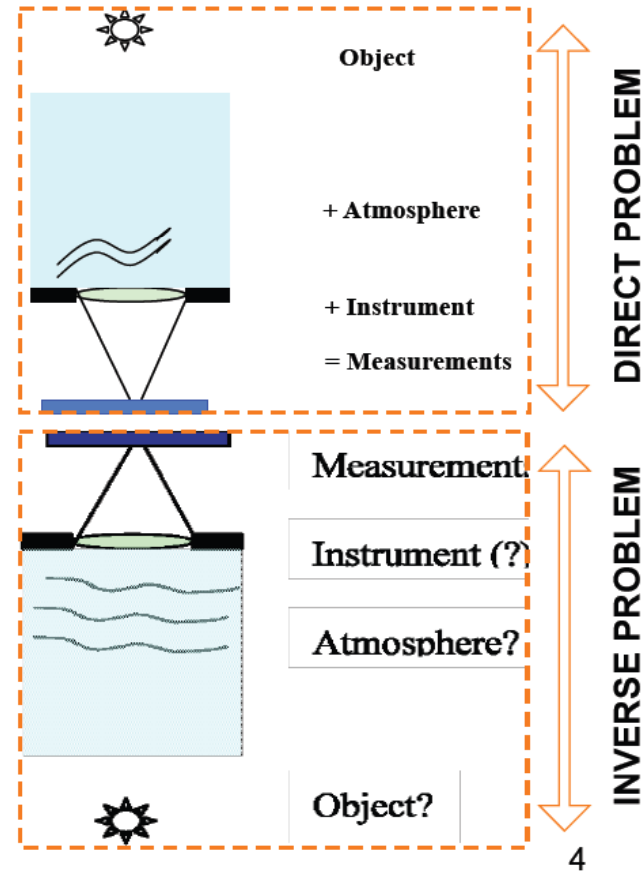
Instantiating a soft core processor within the FPGA enables Matched Filter coefficients calculation on-the-spot.

Imaging through turbulence

- When planar wave-fronts pass through a medium with variable index of refraction they become distorted
- Slopes in the wave-front causes the phase distribution to be stretched like a rubber sheet
- Geometric optics model:



→ Aim is to map the distorted distribution back to uniform



C. Correia et al, Tomography Lecture Series #2 - Feb, 2011

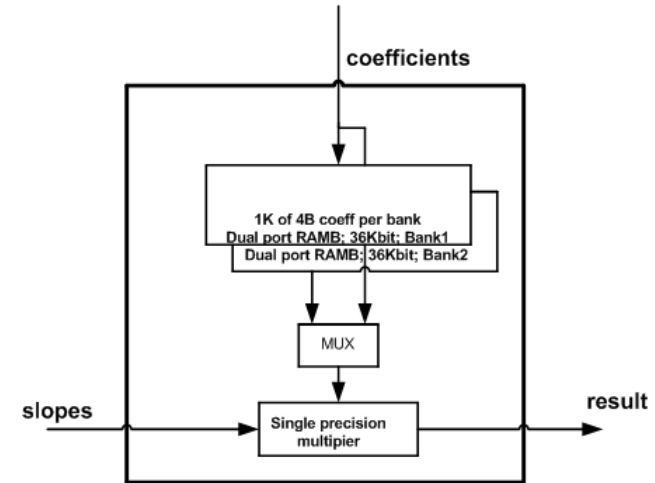
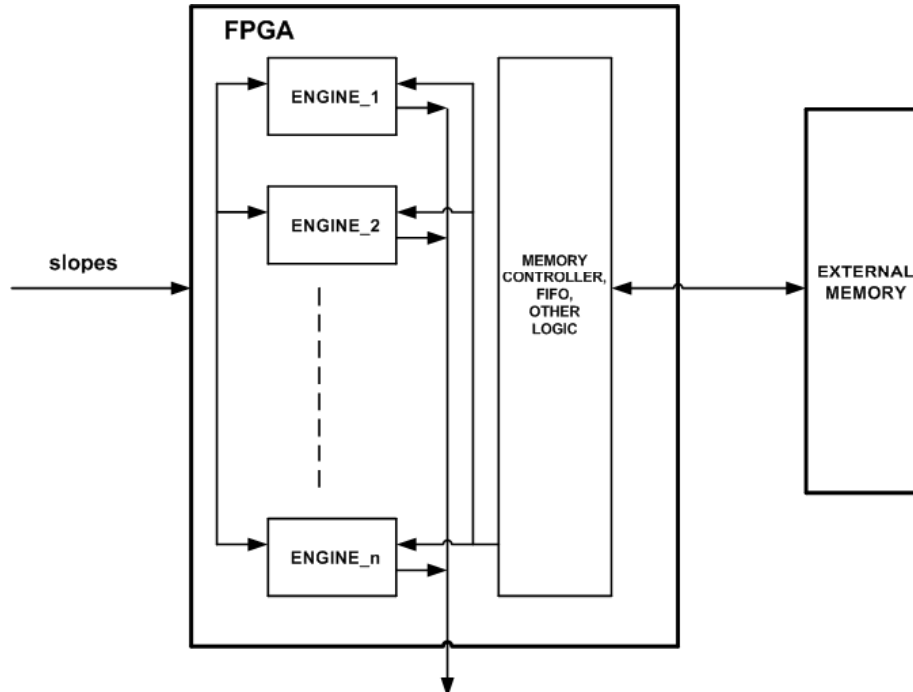
Matrix Vector Multiplication

Computing DM commands directly from slopes:

$$\begin{bmatrix} A_{1,1} & A_{1,2} & A_{1,3} & \dots & A_{1,30984} \\ A_{2,1} & A_{2,2} & A_{2,3} & \dots & A_{2,30984} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ A_{7083,1} & A_{7083,2} & \dots & \dots & A_{7083,30984} \end{bmatrix} \begin{bmatrix} G_1 \\ G_2 \\ \vdots \\ G_{30984} \end{bmatrix} = \begin{bmatrix} A_{1,1}G_1 + A_{1,2}G_2 + A_{1,3}G_3 + \dots + A_{1,30984}G_{30984} \\ A_{2,1}G_1 + A_{2,2}G_2 + A_{2,3}G_3 + \dots + A_{2,30984}G_{30984} \\ \vdots \\ A_{7083,1}G_1 + A_{7083,2}G_2 + A_{7083,3}G_3 + \dots + A_{7083,30984}G_{30984} \end{bmatrix}$$

- There are 30984 slopes vector and 7093 DM actuators.
- Matrix is 30984 X 7083, each element is 4 Bytes, which is 880MB.
- This 2 X 30984 X 7083 Flop = 2 X 219,459,672 Flop ~ 440MFlop.
- For completing the task in 1ms the computing requirements are:
440GFlop/s and 880GB/s memory bandwidth
- The calculation could be done by using many processing engines in parallel.

MVM implementation



- Slopes rate: 31K per 1ms ~ 32ns.
- For each slope processing 4 Bytes of data from ext mem.
- For 100 calculations $400B/32ns = 12.5GB/s$, which is max. Otherwise there are enough DSP slices and RAM Blocks to build 500 engines.
- Memory has to operate in a full page burst mode in order to achieve maximum bandwidth.

- To process all of the slopes we need $7100:100 = 71$ FPGAs, which is 9 Kermode boards system.
- We need 5 Virtex 7 Kermode boards system due to twice the memory bandwidth.
- We need 3 Virtex 8 Kermode boards system due to four times the memory bandwidth.

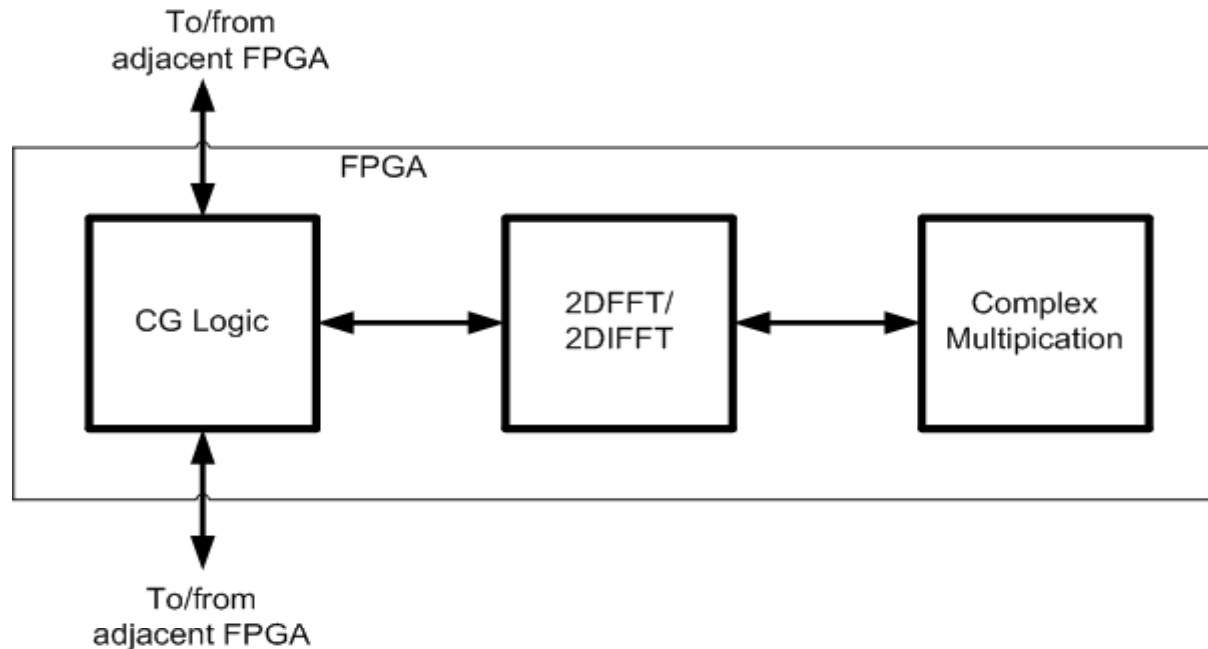
Conjugate Gradient

- This is an iterative method where we first estimate phase points, tomography, and then DM commands, DM fitting.
- A recent study claims that a 20 iteration of Block-Gauss-Seidel-CG20 could be done using one Kermode board in 120 μ s.
- To achieve high data bandwidth between FPGAs on the board special cables are required.
- A 2 Kermode board system with a custom Zone 3 backplane should be able to perform task.

Fourier Domain preconditioned CG algorithm

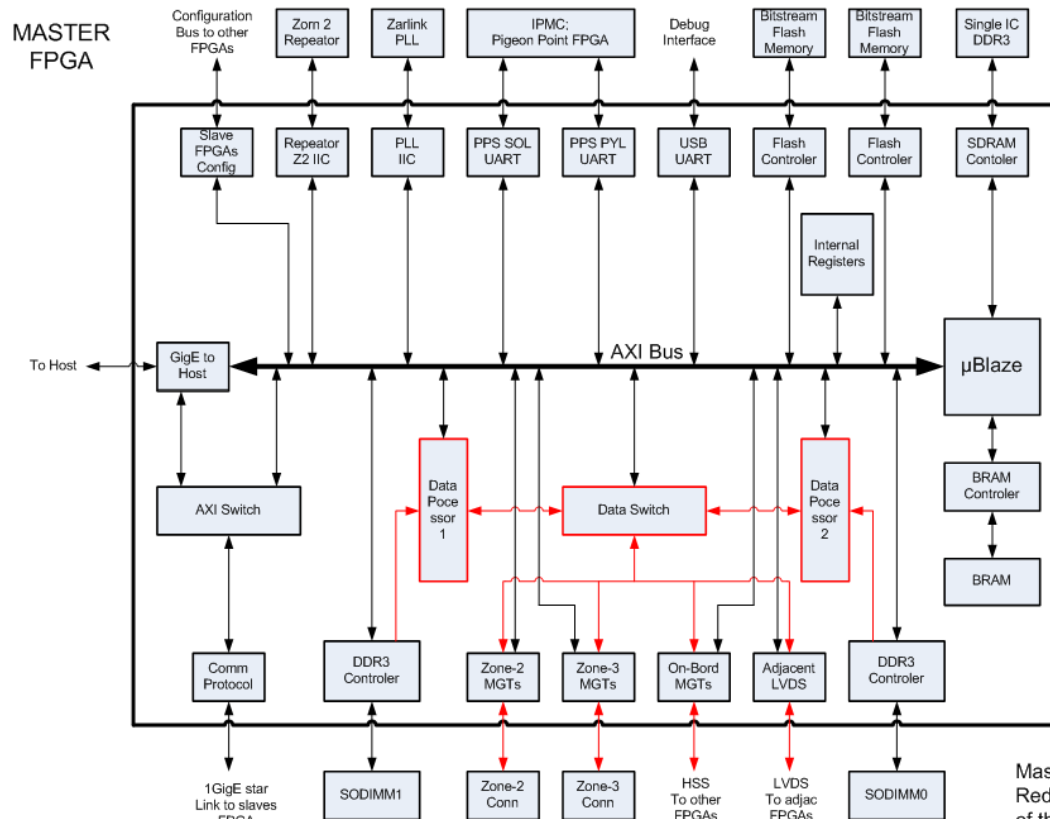
- The latest simulations show that Fourier domain preconditioning combined with Conjugate Gradient algorithm could produce more accurate results and be simpler to implement.
- The algorithm uses 2D FFT with Conjugate Gradient.
- This could be implemented in the Kermode based system.

FD CG Implementation



- Same logic block performs FFT and IFFT.
- 128 point FFT/IFFT takes 700ns. 64 FFT modules will consume 768, out of 2016, DSP slices.
- To 2DFFT 128 X 128 matrix will take $2 \times 2 \times 700\text{ns} = 2.8\mu\text{s}$, the same is the case for 2DIFFT, so in total about $10\mu\text{s}$ to go both direction if we add some data reordering time and if we keep intermediate data in local Block RAM.
- So 3 passes of 2DFFT/IFFT would add $30\mu\text{s}$.
- This leaves enough time and logic for the rest of operations in a 2 Kermode boards system.

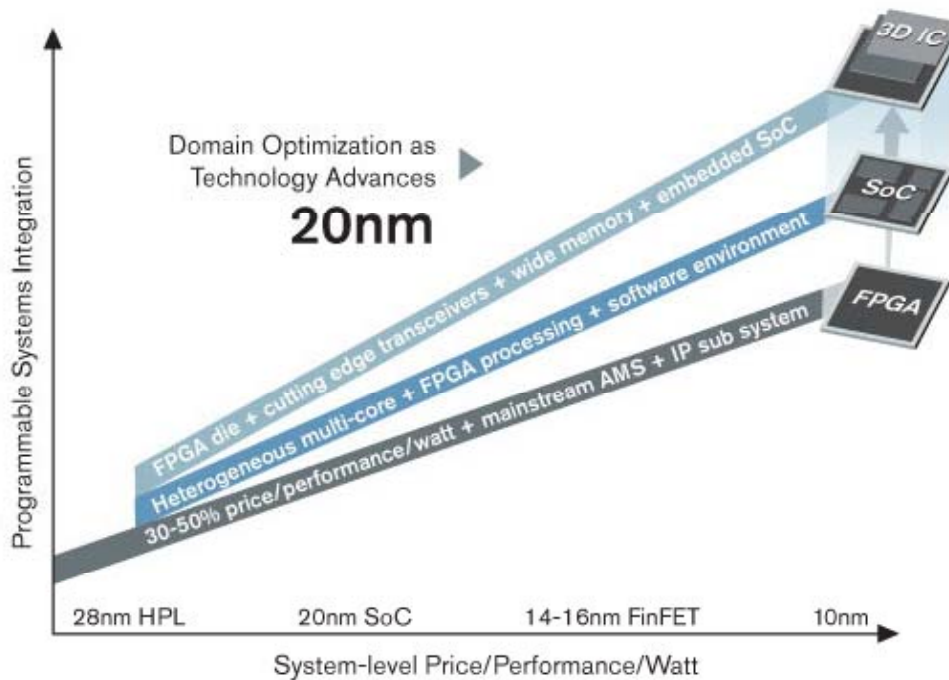
Designing with FPGA challenges



Master FPGA.
Red blocks are parts of the application.
Red lines are data paths.

- The devices have become more capable, and more complex.
- Many IP cores are provided by the vendor, all have to work together in a device.
- AXI bus is all but n-bit bus, different flavors for different tasks.
- Majority of the FPGA infrastructure will be provided by the Board Support Package, BSP, leaving us to deal with red framed boxes only.

Xilinx roadmap



All Programmable 20nm FPGA

Laying the foundation for the rest of the portfolio, the core FPGA combines the 20nm process with a new set of design innovations for Xilinx's 8 series FPGAs. **These next generation devices give another 50% price-performance-per-watt improvement, twice the memory bandwidth and the next generation of industry leading system optimized transceivers.**