RTC Workshop
Dec 5th, 2012

Present Microgate RTCs and perspectives

R. Biasi

Microgate
Outline

- Past and present RTCs applications at Microgate
  - Real time control of AO correctors
  - Real-time reconstructors
  - Slope computers
  - Software aspects
- Lessons learned
- Future perspectives
How it started/ motivations

• Initially designed to control the LBT Adaptive Secondary units

• Motivations for a full custom design:
  • co-existence of digital & analog electronics requirements (capacitive sensors, voice coil motors drivers)
  • dimensional constraints
  • cooling constraints
  • computational performance + diagnostics
  • need for a ‘true parallel’ machine

2003 design...

- Actuators’ cold plate
- Control electronics
- Reference body
- Capacitive sensor armatures
- Magnets
- Thin shell 1.6–2.0mm
- Response time: < 1ms
- Position noise: < 3nm rms @ 40kHz
VLT DSM control electronics

- 13 x DSP control boards

VLT Deformable Secondary Mirror electronics:
- 1170 actuators (capacitive sensor + voice coil motor)
- 156 floating point DSPs
- 3 cooled crates, each comprehending 2 backplanes
- 6 communication boards
- 6 reference signal generation boards
- 30 distribution boards
- 1 Master RT crate
- 1 MG LCU-CPU
Main components: BCU

Fully independent real-time + diagnostic data paths
Main components: DSP control board
Some Hardware...

BCU

1st GEN (LBT) DSP board

2nd Gen (VLT) DSP board
Some Hardware...

- BCU + Xinetics DM interface
- 6-axes CL piezo control
- RTR DSP boards
- VxWorks CPU

Keck NGWFC crate
**BCU**
- 500 MMAC/s floating point sustained
- FPGA for seamless interfacing to various protocols and sensors (S-FPDP, SciMeasure, Andor, Xinetics, ...)
- FPGA performs also hardware acceleration + housekeeping (NIOS)
- Gigabit Ethernet interface (copper or fiber) for diagnostic
- 4x fiber modules up to 2.5 Gbit/s each (FiberChannel, S-FPDP) for real time communication

**DSP board**
- 1 GMAC/s floating point sustained (LBT: 84 boards, 84 GMAC/s) – AD DSP TS101
- FPGA for data routing (DMA from/to DSPs, bulk memory access, NIOS embedded controller)

**Gen 2 DSP board (VLT DSM)**
- 2 GMAC/s floating point sustained (VLT: 78 boards, 156 GMAC/s) – AD DSP TS201
- FPGA for data routing (DMA from/to DSPs, bulk memory access, NIOS embedded controller)
- 16 controlled channels, capacitive sensors + voice coil motor

**Backplane**
- Up to 15 DSP boards + 1 BCU board per backplane
- Diagnostic bus: 2 Gbit/s – Real-time bus: 4 Gbit/s (SLVDS)
Contactless Deformable Mirror control

- Co-located control loop
- Global Feedforward
- Shell safety checks (modal forces, stroke, ...)

\[
{F} = [K] \{x\}
\]

PD digital controller

Current driver

Voice Coil Motor

Plant (thin shell)

Diag

Mirror commands (from RTC)

Co-located control typical computational time:

2.5 µs (LBT: 4ch/DSP, VLT: 8ch/DSP)

WFS loop frequency (~ 1kHz)

co-located loop frequency (~ 70kHz)
Main Applications

Real time reconstructor

- LBT + Magellan: RTR implemented in the same boards performing the mirror control
- Keck: dedicated boards for RTR only
- MMT Laser Guide Star Real Time Reconstructor

\[
\Delta m_i = [B]_0 \{S\}_i + ...[B]_n \{S\}_i \Delta m_{i-1} - ...[A]_m \{\Delta m\}_{i-m}
\]

\[
\Delta p_i = [m2p] \{\Delta m\}_i
\]

- LBT: 3 zeros, 3 poles full state (672 d.o.f) MIMO filter
**RTR Performances**

**LBT**
RTR + Global DM control + shell safety: **260µs**

**Keck**
RTR + TT & DM update: **110µs**

**VLT**
RTR + Global DM control + shell safety: **130µs**
Slope computers

- Flexible system, can be configured for pyramid and SH wavefront sensors by reprogramming a LUT
- Pipelined operation: zero latency for all implemented cases, including pyramid
- Interfaced to several CCD controllers and CCDs: SciMeasure CCD39, CCDi56, CCD50, Andor, …
Main Applications

Slope computer for the LBT ARGOS LGS system

- Includes 8 high speed, very low noise ADC acquisition channels (pnCCD)
- 3x SH implementation, 264x264 pixels, 3x200 8x8 pixel subaps
- Almost fully pipelined operation, 50 μs latency after last pixel acquisition
Software

- Hard real-time DSP software runs without operating system (ISR + main loop)
- Synchronization through real-time communication
- One BCU acts as arbiter and controls ‘data recirculation’ for parallel processing
- Deterministic timing with extremely low jitter, sub-microsecond level
- Very efficient real-time diagnostic buffering system, implemented on hardware
- Real-time system ‘hidden’ behind a host machine interfaced by standard Ethernet
  - LBT: Linux workstation (designed and implemented by INAF-Arcetri)
  - Keck and VLT: single board computer running under VxWorks
- Low-level communication based on simple read-write protocol with direct access to all embedded devices (DSPs, FPGA, bulk memory)
E-ELT M4 deformable mirror control unit

- Line Replaceable Unit comprehending ~30 actuators, control electronics and supply
- Global control moved away from adaptive unit
  → on-board power minimized
- Simplified interfaces and harness (supply, data, cooling)
- Sound maintenance concept, maximize system availability

- FPGA-based local control
  - Parallel/pipelined implementation
  - Minimum latency, ~400ns control loop computational delay, 36ch controlled by one single FPGA
Lessons learned

• Positive experience with dedicated electronics
  (is it really custom? More than 500 MIC DSP boards produced…)

• COTS are not trouble-free and support over system lifetime can be an issue

• Expandability, true parallel architecture, very efficient data recirculation are mandatory for demanding processing application (real world is never just a matrix-vector multiply…)

• Hardware acceleration is appealing but development/debugging time shall not be underestimated (FPGA vs. DSP, HW vs. SW)

• Diagnostic/telemetry tasks shall be carefully evaluated – need for independent paths for real-time and diagnostic communication

• Importance of an abstraction layer to hide the hardware complexity and to define a clear interface to the other layers (e.g., VLT WFM with VLT TCS and SPARTA)
• The Contactless Deformable Mirror control electronics development remains an important niche for Microgate (it’s not only real time processing…)

• For ELT-class DMs, with several thousands of actuators, it is more effective to de-localize the global DM control computation (motivations: on-board dissipation, well-defined modular design, maintainability, …) → comparable problem and complexity of AO RTR

• We also intend to remain in the AO RTC field

• Therefore, we are about starting a development project (partially founded by ProvBZ), with the goal of implementing an acceleration hardware, hosted on standard PCs, with a flexible and modular software approach, and well aligned with the ELTs standard interfaces. Detailed workplan still under definition

• Project team:
  • Microgate
  • Politecnico di Milano – Dipartimento di Ingegneria Aerospaziale (prof. Morandiun)
  • Industrial Mathematics Institute, Johannes Kepler University Linz (prof. Bamltu)
We want to stay on board… so we are here to learn!