The SPARTA Platform: Design, Status and Perspectives

Marcos Suárez Valles
Adaptive Optics Systems (ESO)
msuarez@eso.org
SPARTA Platform Targets

- **ESO Standard Platform for Adaptive Optics Real-Time Applications**
- **SPARTA instrument portfolio:**
  - High-order, low-noise SCAO/XAO/GLAO
  - Low-order, low-noise SCAO

<table>
<thead>
<tr>
<th>Loop Rate</th>
<th>WFS</th>
<th>Detector</th>
<th>WFS Size</th>
<th>Subap. Size</th>
<th># Subap.</th>
<th>Pixel Rate</th>
<th># DM</th>
<th># Actuators</th>
<th>Complexity</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPHERE</td>
<td>1.2 kHz</td>
<td>CCD220</td>
<td>SH 40x40</td>
<td>6x6 pixel</td>
<td>1,240</td>
<td>66 MPix/s</td>
<td>1</td>
<td>1,377</td>
<td>5.2 GMAC</td>
</tr>
<tr>
<td>AOF</td>
<td>1 kHz</td>
<td>CCD220</td>
<td>SH 40x40</td>
<td>6x6 pixel</td>
<td>1,240</td>
<td>230 MPix/s</td>
<td>1</td>
<td>1,170</td>
<td>11.8 GMAC</td>
</tr>
<tr>
<td>ERIS</td>
<td>1.2 kHz</td>
<td>CCD220</td>
<td>PY 40x40</td>
<td>6x6 pixel</td>
<td>1,256</td>
<td>66 MPix/s</td>
<td>1</td>
<td>1,170</td>
<td></td>
</tr>
<tr>
<td>NAOMI</td>
<td>1 kHz</td>
<td>CCD60</td>
<td>5x5</td>
<td>6x6 pixel</td>
<td>36</td>
<td>6.8 Mpix/s</td>
<td>1</td>
<td>49</td>
<td></td>
</tr>
<tr>
<td>GRAVITY</td>
<td>500Hz</td>
<td>SAPHIRA</td>
<td>9x9</td>
<td>4x4 pixel</td>
<td>62</td>
<td>3.3 Mpix/s</td>
<td>1</td>
<td>60</td>
<td></td>
</tr>
</tbody>
</table>

**SPHERE 41x41 HO DM grid:**
- 1,377 used actuators

**CCD220 240x240 pixel frame:**
- 1,240 used subapertures
SPARTA Real-Time Computer

Co-processing Cluster
- Multi-CPU, multi-core Linux nodes
- RTC component logic co-ordination
- Loop parameters configuration
- Distributed telemetry data processing
- RTC calibration logic/algorithms

Real-Time Box
- Hybrid CPU/DSP+FPGA nodes
- Switched VXS communication fabrics
- Low-latency WFS and actuator I/F
- Loop closure/disturbance injection
- Loop-rate telemetry data publication

---

Curtiss-Wright VPF1:
- 2 x 744x PowerPC CPUs (1GHz)
- 2 x Virtex Pro-II FPGAs (125MHz)

Bittware T2V6:
- 2 x TS201 DSP clusters (600MHz)
- 2 x Virtex-II Pro FPGAs (125MHz)

Curtiss-Wright CSW1:
- Zero-latency circuit switching
- 14 x 3.215Gbps VXS Links (4x)
Real-Time Box Pipeline

Wavefront processing:
- Weighted Centre of Gravity (WCoG)

Wavefront reconstruction:
- Matrix-Vector-Multiplication (MVM)

Command time filtering (control):
- Infinite-Impulse-response (IIR) filter
- DM saturation management (anti-windup)
- DM garbage collection
- DM disturbance injection

\[
\begin{align*}
    s_{x/y} &= \frac{\sum w_i \cdot p_i \cdot x_i / y_i}{\sum w_i \cdot p_i} \\
    \ddot{u}_n &= M \cdot \ddot{s}_n \\
    \ddot{y}_n &= b_0 \cdot \ddot{u}_n + \dddot{K}_{n/n-1}
\end{align*}
\]
Real-Time Box Processing Nodes

- WCoG in parallel with WFS readout
- Block-wise reconstruction in parallel with WCoG
- Time filtering in parallel with data transfer
- Loop telemetry/disturbance in idle time

The SPARTA Platform: Design, Status and Perspectives | 05.12.2012
Real-Time Box Processing Nodes

- WCoG in parallel with WFS readout
- Block-wise reconstruction in parallel with WCoG
- Time filtering in parallel with data transfer
- Loop telemetry/disturbance in idle time
Real-Time Box Performance

- **SPHERE overall end-to-end latency:** ~80μs
  - FPGA wavefront processing latency: ~2 μs
  - DSP reconstruction latency: ~40 μs
  - FPGA HO command filtering: ~17 μs
  - CPU TT command filtering: ~38 μs

CPU bounded
Co-processing Cluster Performance

- DDS confirmed reliability QoS (no packet loss)
- IP multicast over IGMP-enabled switch
- Loop concentrator performance:

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Size</th>
<th>Throughput</th>
<th>CPU usage (*)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPHERE</td>
<td>1.2 kHz</td>
<td>20 kB</td>
<td>~24 MB/s</td>
</tr>
<tr>
<td>AOF</td>
<td>1 kHz</td>
<td>67 kB</td>
<td>~66 MB/s</td>
</tr>
</tbody>
</table>

Number crunching performance:

<table>
<thead>
<tr>
<th>Period</th>
<th># Samples</th>
<th>CPU usage (*)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modal Gain Optimisation</td>
<td>30 s</td>
<td>4,096</td>
</tr>
<tr>
<td>Atmospheric Statistics</td>
<td>15 s</td>
<td>4,096</td>
</tr>
</tbody>
</table>

(*) 2 x Xeon 5670 6-core CPU (2.93GHz)
12 GB DDR3 RAM
Co-processing Cluster Software

- Largest part of the SPARTA code base → portability/reusability
  - C++/Linux-based OS (Scientific Linux), no RT patches
  - CORBA (ACE/TAO) for scalable, distributed coordination
  - DDS (RTI) for scalable, distributed data processing
  - Intel MKL for portable, scalable performance
  - MATLAB MCR for complex algorithm portability
  - Minimum number of I/Fs to Real-Time Box, confined in low-level tier
Real-Time Box Software

- Smallest share of the SPARTA code base
- Proportionally largest coding/testing effort
  - C++/RTOS-based (vxWorks)
  - Strongly vectorised (Altivec), loop-unrolled code
  - Zero-copy, in-place data processing (Transcomm)
  - Pluggable, self-contained I/O and processing stages encapsulate HW-specifics
  - Compile-time stage composition and static polymorphism for maximum decoupling

The SPARTA Platform: Design, Status and Perspectives | 05.12.2012
Cluster and Real-Time Box strongly decoupled → may be reused separately
  - Low-impact cluster connection to other RTC pipelines (e.g. workstation-based)

Cluster scalable to great extent:
  - May be collapsed into a single node → SPARTA-Light
  - Or extended to serve bigger E-ELT AO instruments

Cluster employs standard I/Fs and middleware:
  - Inter-operable with other DDS/CORBA-enabled systems/instruments

HW-dependencies in Real-Time Box SW strongly encapsulated:
  - Low-impact porting to workstation environment
  - Low-impact porting to non-FPGA architectures → SPARTA-Light
SPARTA Future Plans (I)

- Switched network RTC interconnects:
  - 10/40/100GbE links
  - UDP protocol potentially running RTPS (DDS interoperability)
  - Layer 2, cut-thru switch: forwarding and reception in parallel
  - Full-duplex, isolated, P2P connections: no collision domain
  - Optimised switch configurations for 1:n and n:1 topologies

- Current 1:1 scale prototypes demonstrate:
  - Deterministic, low latency end-to-end data propagation
  - Repeatable, out-of-order packet delivery in n:1 topology
SPARTA Future Plans (II)

- Multi-CPU, multi-core Real-Time Box nodes:
  - FPGA-aided I/O: preserve GbE real-time capability

- Block-wise, multi-thread vector computation
- vxWorks for intel IA64 required?

- Off-line/online GPU computing engine
- Direct FPGA - GPU data transfers possible?
- In-socket FPGA stacks replacing some CPUs?
Thanks for your attention!

Questions?